1Gb NAND FLASH

1Gb (128Mx 8), 3.3v ,8 bit ECC NAND flash

General Description

The ZDND1GXXXXX is a single 3.3v 1Gbit NAND Electrically Erasable and Programmable Read-Only Memory (NAND E2PROM) organized as (2048 + 128) bytes × 64 pages × 1024 blocks. The device has a 2176-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 2176-byte increments. The Erase operation is implemented in a single block unit (128 Kbytes + 8 Kbytes: 2176 bytes × 64 pages).

The ZDND1GXXXXX is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

Features

- **Single Level per Cell (SLC) Technology**
- **ECC requirement: 8bit/512Bytes**
- **Power Supply Voltage**

  Voltage range: 2.7V ~ 3.6V
- **Organization**

  Page size: x8 (2048 + 128) bytes; 128- bytes spare area

  Block size: x8 (128k + 8k) bytes

  1004 block (min) ~ 1024 block (max)
- **Modes**

  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy
- **Access time**

  Cell array to register: 25µs (max)

  Serial Read Cycle: 25 ns (min) (CL=50pF)
- **Program/Erase time**

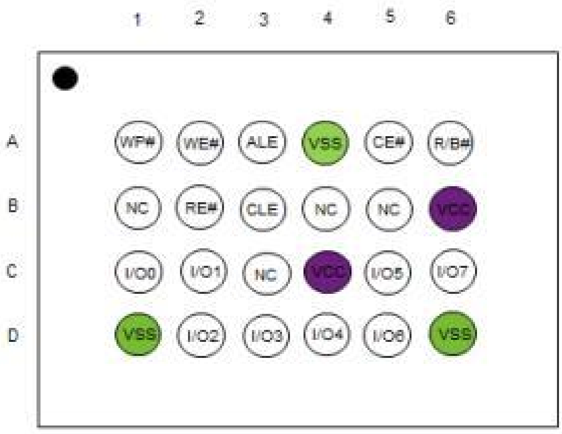
  Auto Page Program: 300 µs /page (typ.)

  Auto Block Erase: 2.5 ms/block(typ.)
- **Reliability**

  10 Year Data retention (Typ)

Pin Assignments

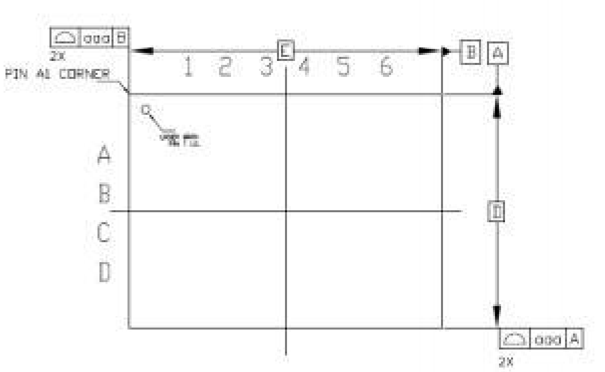
Ball down , top view



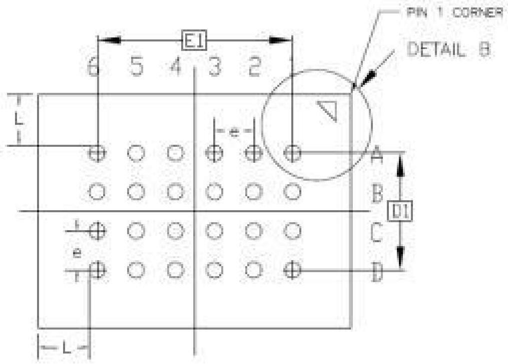
BGA24, 6x8x1mm, ball pitch 1.0

Supply Ground

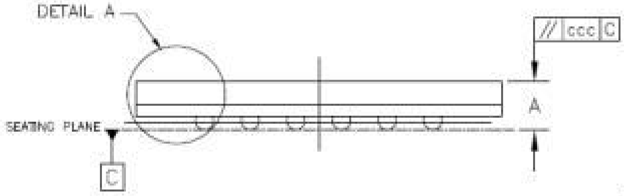
Package Dimension



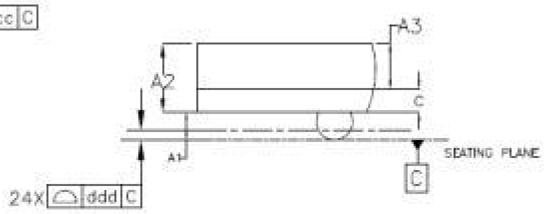
TOP VIEW



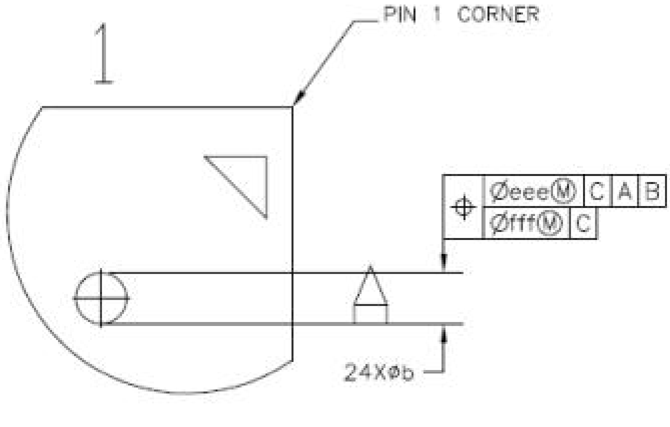
BOTTOM VIEW



SIDE VIEW



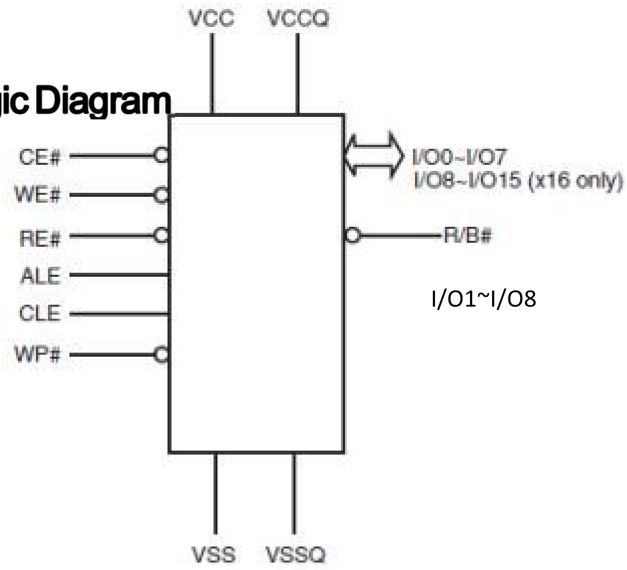
DETAIL A(2:1)



DETAIL B(2:1)

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.14
A1	0.25	0.30	0.35
A2	0.71	0.76	0.81
A3	0.50 BASIC		
c	0.22	0.26	0.30
D	5.90	6.00	6.10
D1	3.00 BASIC		
E	7.90	8.00	8.10
E1	5.00 BASIC		
e	1.00 BASIC		
b	0.35	0.40	0.45
L	1.30 REF		
ddd	0.10		
ccc	0.15		
ddd	0.10		
eee	0.15		
fff	0.10		

Logic Diagram



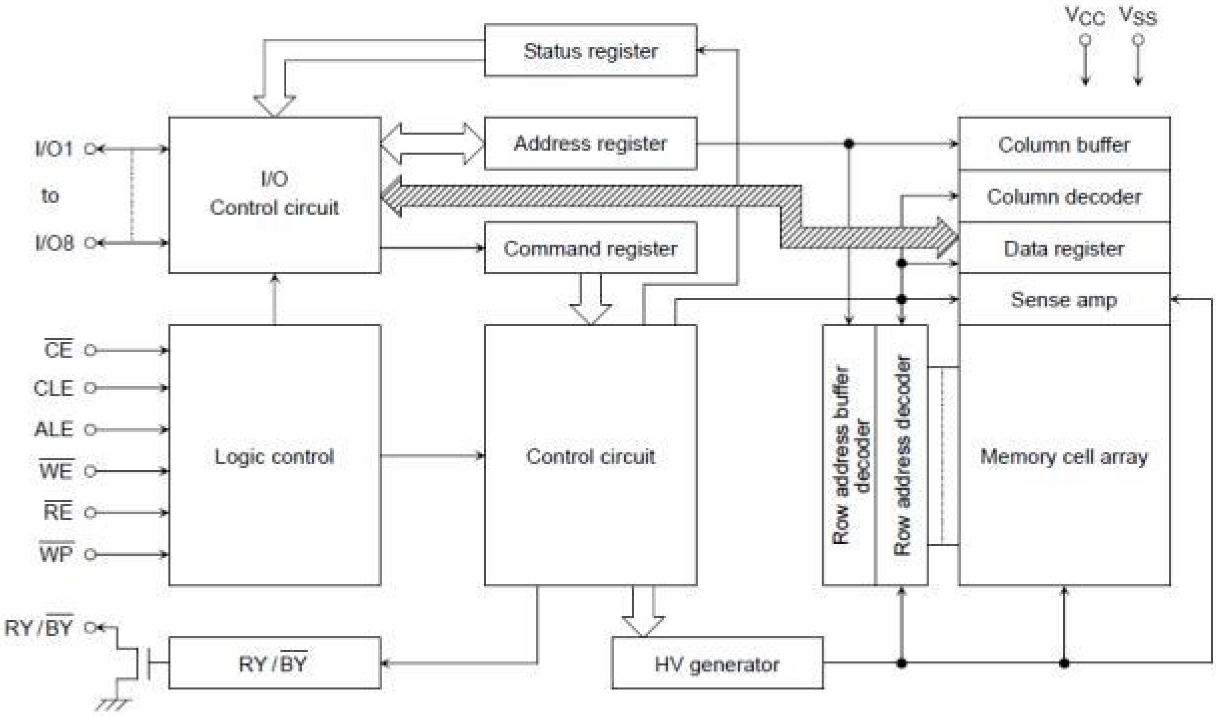
Pin Description

Pin Name	Description
I/O1 - I/O8 (x8)	**Inputs/Outputs**. The I/O pins are used for command input, address input, data input, and data output. The I/O pins float to High-Z when the device is deselected or the outputs are disabled.
CLE	**Command Latch Enable.** This input activates the latching of the I/O inputs inside the Command Register on the rising edge of Write Enable (WE#).
ALE	**Address Latch Enable.** This input activates the latching of the I/O inputs inside the Address Register on the rising edge of Write Enable (WE#).
CE#	**Chip Enable.** This input controls the selection of the device. When the device is not busy CE# low selects the memory.
WE#	**Write Enable.** This input latches Command, Address and Data. The I/O inputs are latched on the rising edge of WE#.
RE#	**Read Enable.** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WP#	**Write Protect.** The WP# pin, when low, provides hardware protection against undesired data modification (program / erase).
R/B#	**Ready Busy**. The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	**Supply Voltage**. The VCC supplies the power for all the operations (Read, Program, Erase). An internal lock circuit prevents the insertion of Commands when VCC is less than VLKO.
VSS	**Ground.**
NC	**Not Connected.**

Notes:

1. *A 0.1 µF capacitor should be connected between the VCC Supply Voltage pin and the VSS Ground pinto decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.*

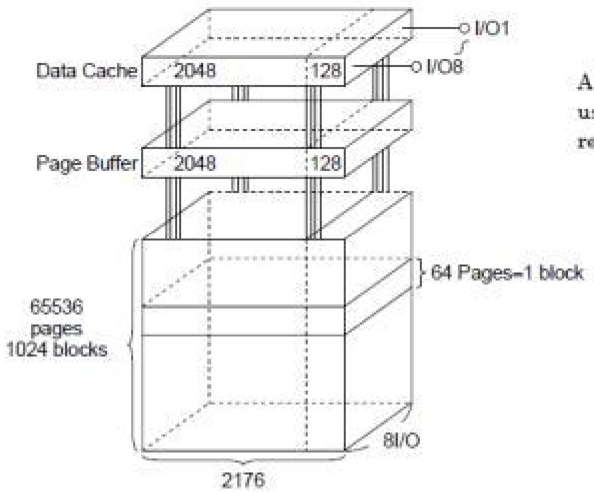
Block Diagram



Array Organization

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.



A page consists of 2176 bytes in which 2048 bytes are used for main memory storage and 128 bytes are for redundancy or for other uses.

1 page = 2176 bytes
1 block = 2176 bytes × 64 pages = (128K + 8K) bytes
Capacity = 2176 bytes × 64pages × 1024 blocks

An address is read in via the I/O port over four consecutive clock cycles, as shown in Table 1.

Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	L	L	CA11	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8

CA0 to CA11: Column address
PA0 to PA15: Page address

PA6 to PA15: Block address
PA0 to PA5: NAND address in block

Absolute Maximum Ratings

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input /Output Voltage	−0.6 to V_{CC} + 0.3 (≤ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	−55 to 150	°C
T_{OPR}	Operating Temperature	-40 to 85	°C

Capacitance *(Ta = 25°C, f = 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.

Valid Blocks

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	1004	—	1024	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document. The first block (Block 0) is guaranteed to be a valid block at the time of shipment. The specification for the minimum number of valid blocks is applicable over lifetime The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

Recommended DC Operating Conditions

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	2.7	—	3.6	V
V_{IH}	High Level input Voltage	Vcc x 0.8	—	VCC + 0.3	V
V_{IL}	Low Level Input Voltage	−0.3*	—	Vcc x 0.2	V

* -2 V (pulse width lower than 20 ns)

DC Characteristics (Ta = -40 to 85℃, VCC = 2.7 to 3.6V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO1}	Serial Read Current	CE# = V_{IL}, I_{OUT} = 0 mA, tcycle = 25	—	—	30	mA
I_{CCO2}	Programming Current	—	—	—	30	mA
I_{CCO3}	Erasing Current	—	—	—	30	mA
I_{CCS}	Standby Current	CE# = V_{CC}−0.2 V, WP# = 0 V/V_{CC}	—	—	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = −0.1 mA	Vcc - 0.2	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 0.1 mA	—	—	0.2	V
I_{OL} (RY/BY)	Output current of RY/BY pin	V_{OL} = 0.2 V	—	4	—	mA

AC CHARACTERISTICS AND RECOMMENDED OPERATING

(Ta = -40 to 85℃, VCC = 2.7 to 3.6V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
tCLS	CLE Setup Time	12	—	ns
tCLH	CLE Hold Time	5	—	ns
tCS	CE# Setup Time	20	—	ns
tCH	CE# Hold Time	5	—	ns
tWP	Write Pulse Width	12	–	ns
tALS	ALE Setup Time	12	–	ns
tALH	ALE Hold Time	5	—	ns
tDS	Data Setup Time	12	—	ns
tDH	Data Hold Time	5	–	ns
tWC	Write Cycle Time	25	–	ns
tWH	WE# High Hold Time	10	—	ns
tWW	WP# High to WE# Low	100	—	ns
tRR	Ready to RE# Falling Edge	20	–	ns
tRW	Ready to WE# Falling Edge	20	–	ns
tRP	Read Pulse Width	12	—	ns
tRC	Read Cycle Time	25	—	ns
tREA	RE# Access Time	–	20	ns
tCEA	CE# Access Time	–	25	ns
tCLR	CLE Low to RE# Low	10	—	ns
tAR	ALE Low to RE# Low	10	—	ns
tRHOH	RE# High to Output Hold Time	25	–	ns
tRLOH	RE# Low to Output Hold Time	5	–	ns
tRHZ	RE# High to Output High Impedance	–	60	ns
tCHZ	CE# High to Output High Impedance	—	20	ns
tCSD	CE# High to ALE or CLE Don't Care	0	–	ns
tREH	RE# High Hold Time	10	–	ns
tIR	Output-High-impedance-to- RE# Falling Edge	0	—	ns
tRHW	RE# High to WE# Low	30	—	ns
tWHC	WE# High to CE# Low	30	–	ns
tWHR	WE# High to RE# Low	60	–	ns
tR	Memory Cell Array to Starting Address	–	25	µs
tDCBSYR1	Data Cache Busy in Read Cache (following 31h and 3Fh)	–	25	µs
tDCBSYR2	Data Cache Busy in Page Copy (following 3Ah)	—	30	µs
tWB	WE# High to Busy	—	100	ns
tRST	Device Reset Time (Ready/Read/Program/Erase)	–	5/5/10/500	µs

*1: tCLS and tALS can not be shorter than tWP

*2: tCS should be longer than tWP + 8ns.

AC Test Conditions

PARAMETER	CONDITION
	V_{CC}: 2.7 to 3.6V
Input level	V_{CC} - 0.2 V, 0.2 V
Input pulse rise and fall time	3 ns
Input comparison level	Vcc / 2
Output data comparison level	Vcc / 2
Output load	C_L (50 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the RY/BY# pin.

Programming and Erasing Characteristics

(Ta = -40 to 85℃, V_{CC} = 2.7 to 3.6V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time	—	300	700	µs	
$t_{DCBSYW2}$	Data Cache Busy Time in Write Cache (following 15h)	—	—	700	µs	(1)
N	Number of Partial Program Cycles in the Same Page	—	—	4		
t_{BERASE}	Block Erasing Time	—	2.5	5	ms	

(1) tDCBSYW2 depends on the timing between internal programming time and data in time.

Data Output

When tREH is long, output buffers are disabled by /RE=High, and the hold time of data output depend on tRHOH (25ns MIN). On this condition, waveforms look like normal serial read mode.

When tREH is short, output buffers are not disabled by /RE=High, and the hold time of data output depend on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE, ALE, /CE or falling edge of /WE, and waveforms look like Extended Data Output Mode.

Mode Selection

The operation modes such as Program, Erase, Read and Reset are controlled by command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, /CE , /WE , /RE and /WP signals as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L	⎺_⎺↑	H	*
Data Input	L	L	L	⎺_⎺↑	H	H
Address input	L	H	L	⎺_⎺↑	H	*
Serial Data Output	L	L	L	H	⎺_⎺	*
During Program (Busy)	*	*	*	*	*	H
During Erase (Busy)	*	*	*	*	*	H
During Read (Busy)	*	*	H	*	*	*
	*	*	L	H (*2)	H (*2)	*
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

1. **1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit*
2. **2 :If $\overline{CE}$ is low during read busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read command can be input during Read Busy.*

Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read	00	30	
Column Address Change in Serial Data Output	05	E0	
Read with Data Cache	31	—	
Read Start for Last Page in Read Cycle with Data Cache	3F	–	
Auto Page Program	80	10	
Column Address Change in Serial Data Input	85	—	
Auto Program with Data Cache	80	15	
Read for Page Copy (2) with Data Out	00	3A	
Auto Program with Data Cache during Page Copy (2)	8C	15	
Auto Program for last page during Page Copy (2)	8C	10	
Auto Block Erase	60	D0	
ID Read	90	–	
Status Read	70	—	∘
Reset	FF	–	∘

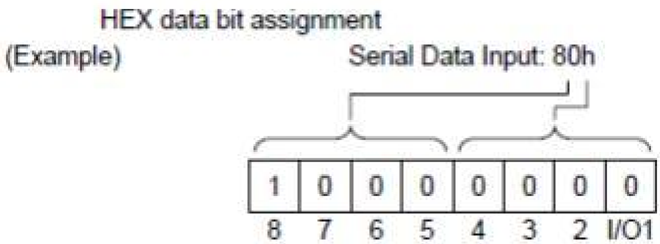


Table 4. Read mode operation states

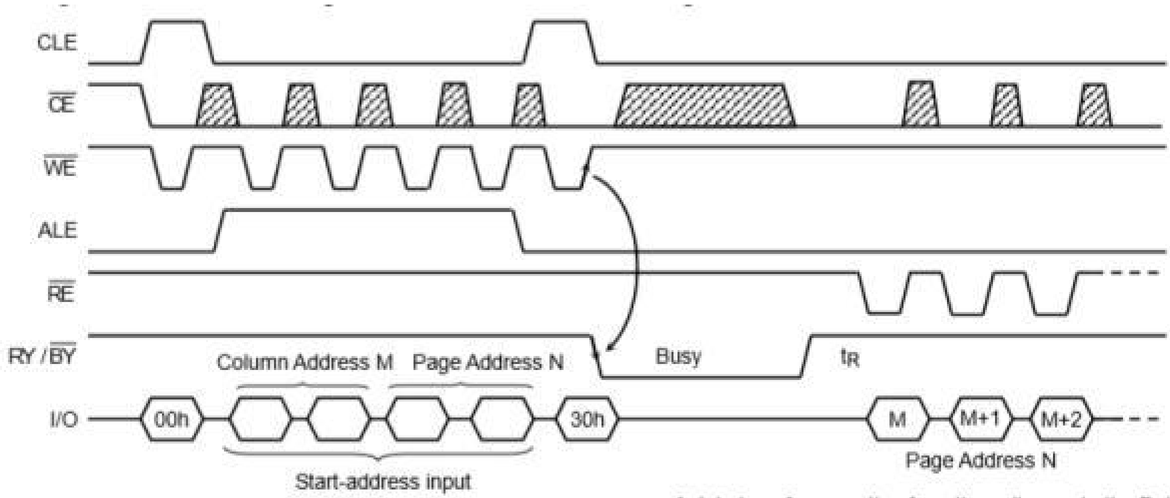
	CLE	ALE	CE	WE	RE	I/O1 to I/O8	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

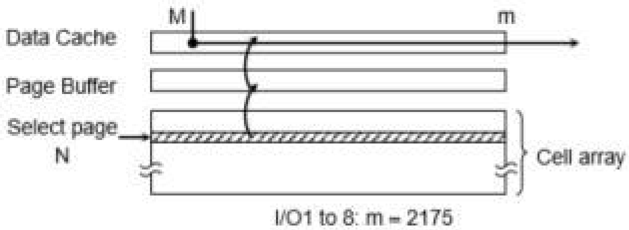
H: VIH, L: VIL

Device Operation

Read Mode

Read mode is set when the "00h" and “30h” commands are issued to the Command register. Between the two commands, a start address for the Read mode needs to be issued. After initial power on sequence, “00h” command is latched into the internal command register. Therefore read operation after power on sequence is executed by the setting of only five address cycles and “30h” command. Refer to the figures below for the sequence and the block diagram (Refer to the detailed timing chart.).

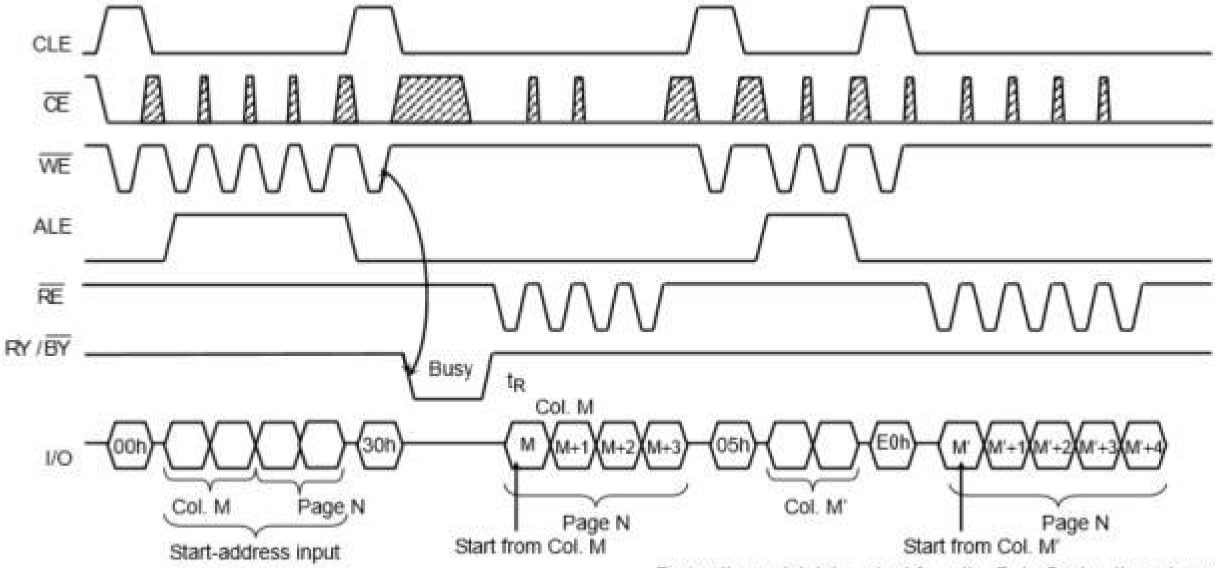


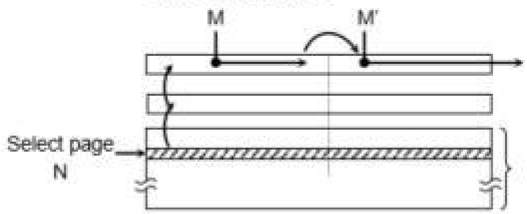


A data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of WE in the 30h command input cycle (after the address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the RE clock from the start address designated in the address input cycle.

Random Column Address Change in Read Cycle

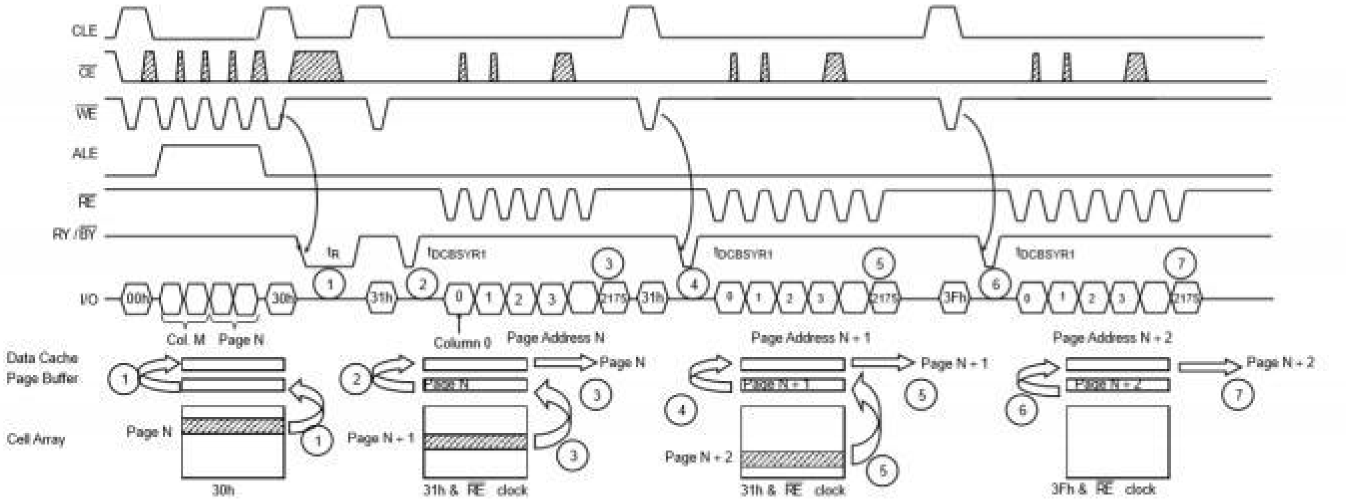




During the serial data output from the Data Cache, the column address can be changed by inputting a new column address using the 05h and E0h commands. The data is read out in serial starting at the new column address. Random Column Address Change operation can be done multiple times within the same page.

Read Operation with Read Cache

The device has a Read operation with Data Cache that enables the high speed read operation shown below. When the block address changes, this sequence has to be started from the beginning.

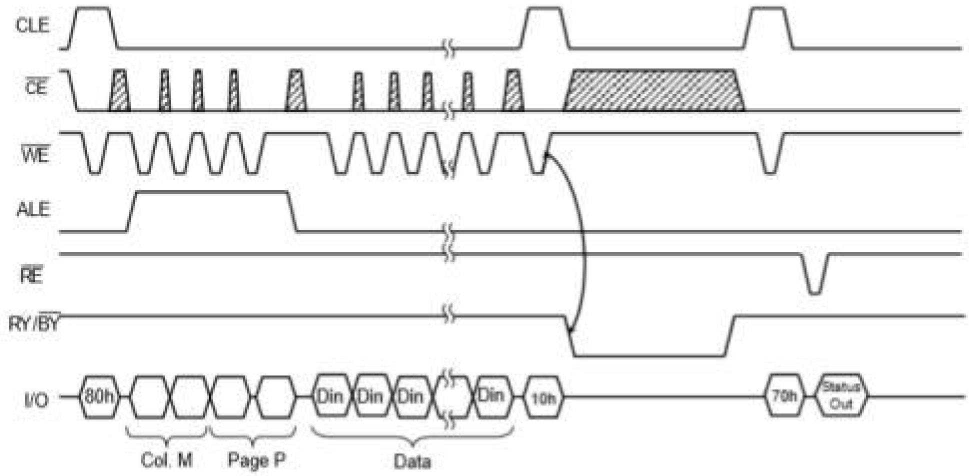


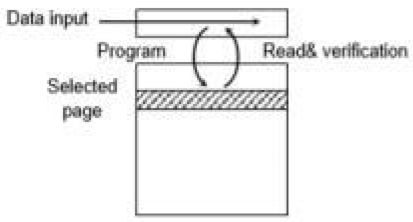
If the 31h command is issued to the device, the data content of the next page is transferred to the Page Buffer during serial data out from the Data Cache, and therefore the tR (Data transfer from memory cell to data register) will be reduced.

1. *Normal read. Data is transferred from Page N to Data Cache through Page Buffer. During this time period, the device outputs Busy state for tR max.*
2. *After the Ready/Busy returns to Ready, 31h command is issued and data is transferred to Data Cache from Page Buffer again. This data transfer takes tDCBSYR1 max and the completion of this time period can be detected by Ready/Busy signal.*
3. *Data of Page N + 1 is transferred to Page Buffer from cell while the data of Page N in Data cache can be read out by /RE clock simultaneously.*
4. *The 31h command makes data of Page N + 1 transfer to Data Cache from Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max.. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.*
5. *Data of Page N + 2 is transferred to Page Buffer from cell while the data of Page N + 1 in Data cache can be read out by /RE clock simultaneously*
6. *The 3Fh command makes the data of Page N + 2 transfer to the Data Cache from the Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max.. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.*
7. *Data of Page N + 2 in Data Cache can be readout, but since the 3Fh command does not transfer the data from the memory cell to Page Buffer, the device can accept new command input immediately after the completion of serial data out.*

Auto Page Program Operation

The device carries out an Automatic Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)



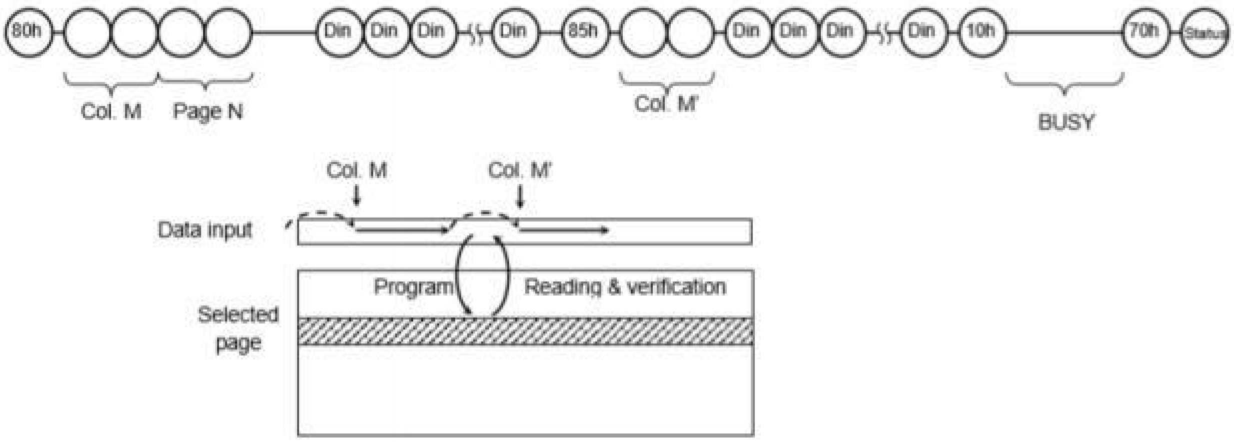


The data is transferred (programmed) from the register to the selected page on the rising edge of WE following input of the "10h" command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Random Column Address Change in Auto Page Program Operation

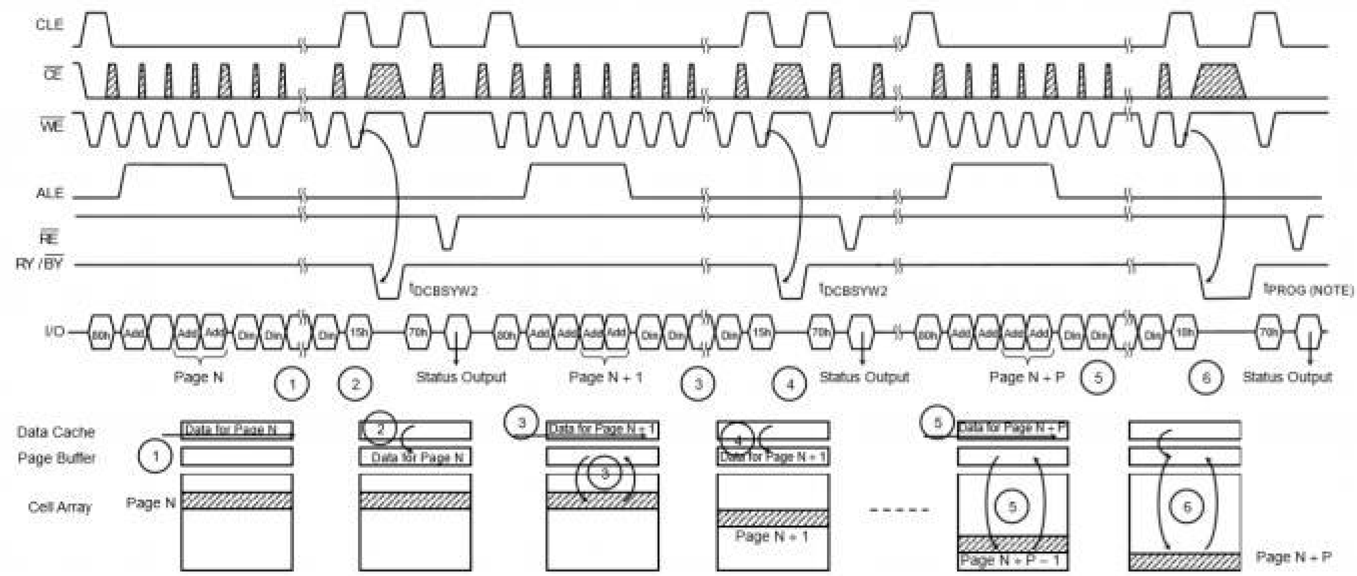
The column address can be changed by the 85h command during the data input sequence of the Auto Page Program operation.

Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.



Auto Page Program Operation with Data Cache

The device has an Auto Page Program with Data Cache operation enabling the high speed program operation shown below. When the block address changes this sequenced has to be started from the beginning



Issuing the 15h command to the device after serial data input initiates the program operation with Data Cache

1. Data for Page N is input to Data Cache.
2. Data is transferred to the Page Buffer by the 15h command. During the transfer the Ready/Busy outputs Busy State (tDCBSYW2).
3. Data is programmed to the selected page while the data for page N + 1 is input to the Data Cache.
4. By the 15h command, the data in the Data Cache is transferred to the Page Buffer after the programming of page N is completed. The device output busy state from the 15h command until the Data Cache becomes empty. The duration of this period depends on timing between the internal programming of page N and serial data input for Page N + 1 (tDCBSYW2).
5. Data for Page N + P isinput to the Data Cache while the data of the Page N + P − 1 is being programmed.
6. The programming with Data Cache is terminated by the 10h command. When the device becomes Ready, it shows that the internal programming of the Page N + P is completed.

NOTE: Since the last page programming by the 10h command is initiated after the previous cache program, the tPROG during cache programming is given by the following;

tPROG = tPROG for the last page + tPROG of the previous page − (command input cycle + address input cycle + data input cycle time of the last page)

Pass/fail status for each page programmed by the Auto Page Programming with Data Cache operation can be detected by the Status Read operation.

. I/O1 : Pass/fail of the current page program operation.

. I/O2 : Pass/fail of the previous page program operation.

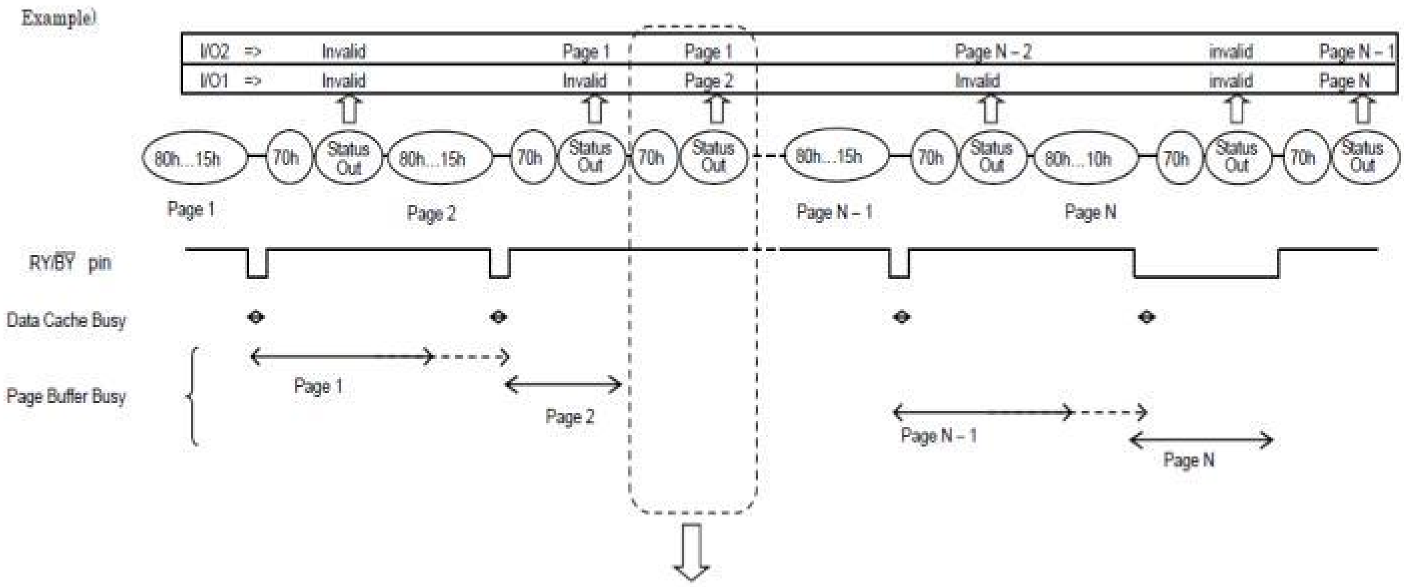
The Pass/Fail status on I/O1 and I/O2 are valid under the following conditions.

. Status on I/O1: Page Buffer Ready/Busy is Ready State.

The Page Buffer Ready/Busy is output on I/O6 by Status Read operation or RY / BY pin after the 10h command

. Status on I/O2: Data Cache Read/Busy is Ready State.

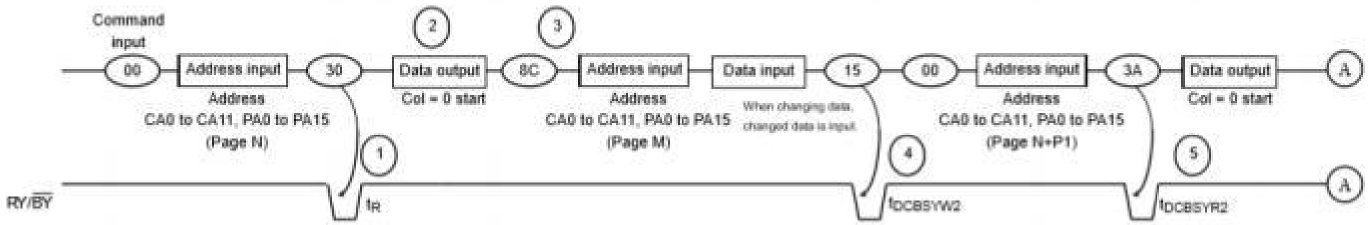
The Data Cache Ready/Busy is output on I/O7 by Status Read operation or RY / BY pin after the 15hcommand.



If the Page Buffer Busy returns to Ready before the next 80h command input, and if Status Read is done during this Ready period, the Status Read provides pass/fail for Page 2 on I/O1 and pass/fail result for Page1 on I/O2

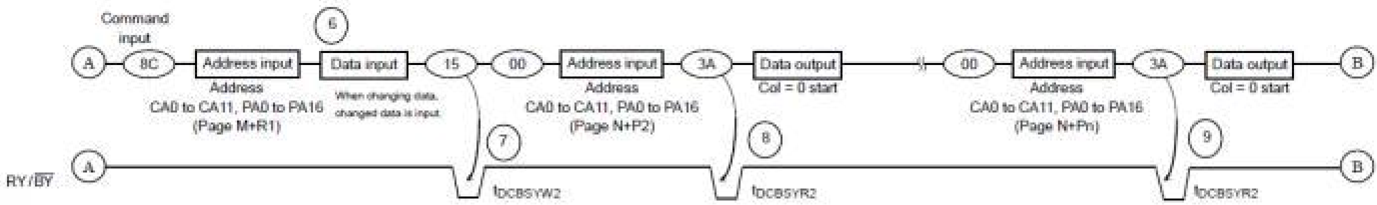
Page Copy (2)

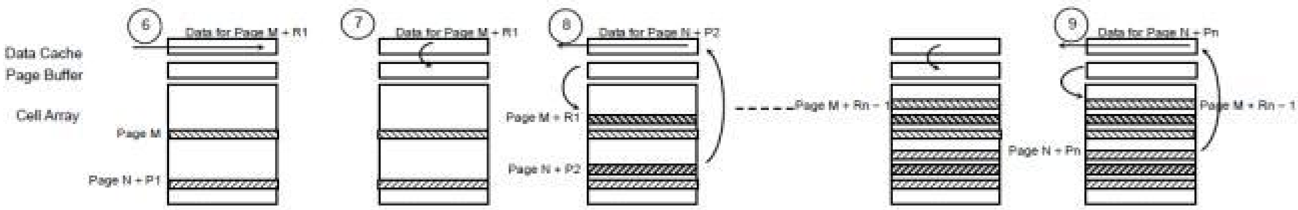
By using Page Copy (2), data in a page can be copied to another page after the data has been readout. When the block address changes (increments) this sequenced has to be started from the beginning.



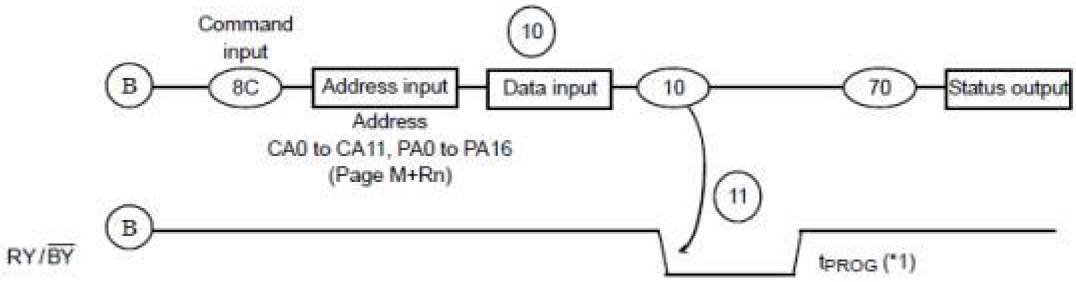
Page Copy (2) operation is as following.

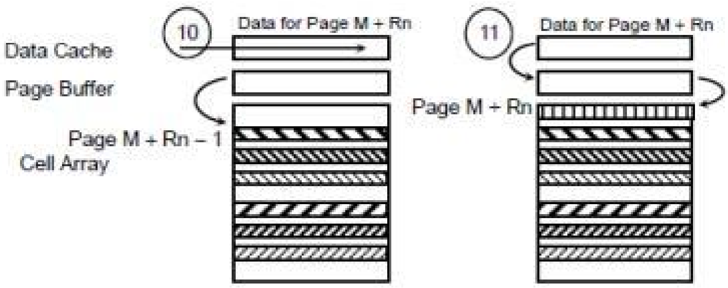
1. Data for Page N is transferred to the Data Cache.
2. Data for Page N is read out.
3. Copy Page address M is input and if the data needs to be changed, changed data is input.
4. Data Cache for Page M is transferred to the Page Buffer.
5. After the Ready state, Data for Page N + P1 is output from the Data Cache while the data of Page M is being programmed.





6. Copy Page address (M + R1) is input and if the data needs to be changed, changed data is input.
7. After programming of page M is completed, Data Cache for Page M + R1 is transferred to the Page Buffer.
8. By the 15h command, the data in the Page Buffer is programmed to Page M + R1. Data for Page N + P2 is transferred to the Data cache.
9. The data in the Page Buffer is programmed to Page M + Rn − 1. Data for Page N + Pn is transferred to the Data Cache.





10. Copy Page address (M + Rn) is input and if the data needs to be changed, changed data is input.

11. By issuing the 10h command, the data in the Page Buffer is programmed to Page M + Rn.

(*1) Since the last page programming by the 10h command is initiated after the previous cache program, the tPROG here will be expected as the following,

tPROG = tPROG of the last page + tPROG of the previous page – (command input cycle + address input cycle + data output/input cycle time of the last page)

NOTE)

Data input is required only if previous data output needs to be altered.

If the data has to be changed, locate the desired address with the column and page address input after the 8Ch command, and change only the data that needs be changed.

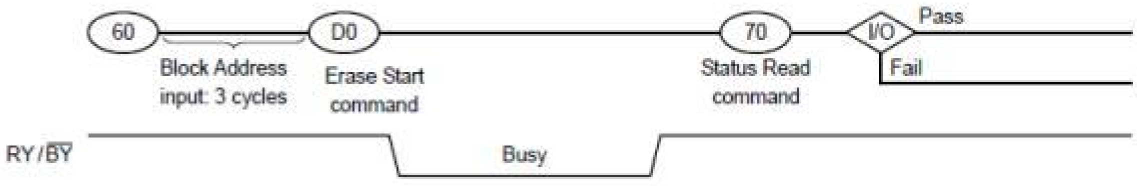
If the data does not have to be changed, data input cycles are not required.

Make sure WP# is held to High level when Page Copy (2) operation is performed.

Also make sure the Page Copy operation is terminated with 8Ch-10h command sequence

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of WE# after the Erase Start command "D0h" which follows the Erase Setup command "60h". This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be readout under the following timing conditions:

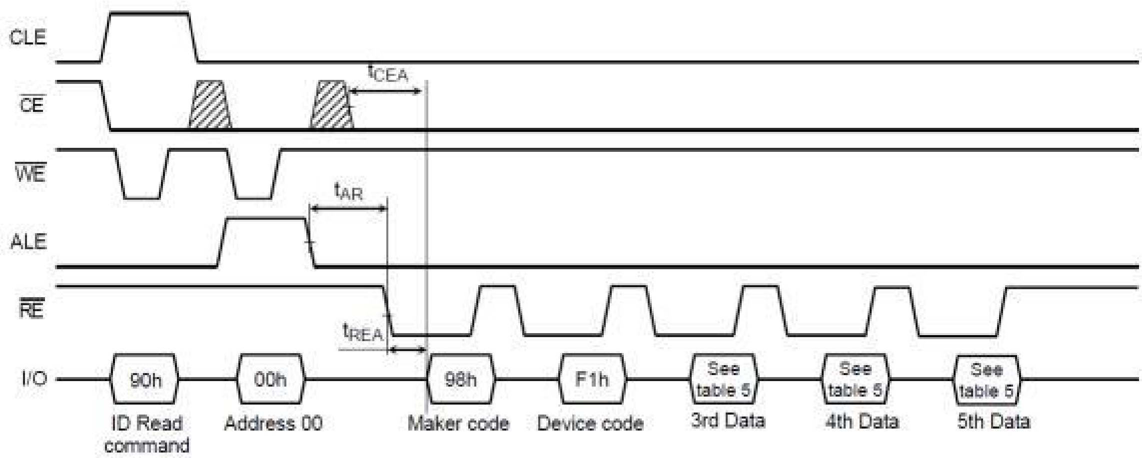


Table 5. Code table

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98h
2nd Data	Device Code	1	1	1	1	0	0	0	1	F1h
3rd Data	Chip Number, Cell Type	1	0	0	0	0	0	0	0	80h
4th Data	Page Size, Block Size, I/O Width	0	0	0	1	0	1	0	1	15h
5th Data	Plane Number	0	1	1	1	0	0	1	0	72h

3rd Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 level cell					0	0		
	4 level cell					0	1		
	8 level cell					1	0		
	16 level cell					1	1		
Reserved		1	0	0	0				

4th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Page Size	1 KB							0	0
	2 KB							0	1
(without redundant area)	4 KB							1	0
	8 KB							1	1
Block Size	64 KB			0	0				
	128 KB			0	1				
(without redundant area)	256 KB			1	0				
	512 KB			1	1				
I/O Width	x8		0						
	x16		1						
Reserved		0				0	1		

5th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Plane Number	1 Plane					0	0		
	2 Plane					0	1		
	4 Plane					1	0		
	8 Plane					1	1		
Reserved		0	1	1	1			1	0

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass /fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using RE# after a “70h” command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status.

The resulting information is outlined in Table 6.

Table 6. Status output table

	Definition	Page Program Block Erase	Cache Program	Read Cache Read
I/O1	Chip Status1 Pass: 0 Fail: 1	Pass/Fail	Pass/Fail	Invalid
I/O2	Chip Status 2 Pass: 0 Fail: 1	Invalid	Pass/Fail	Invalid
I/O3	Not Used	0	0	0
I/O4	Not Used	0	0	0
I/O5	Not Used	0	0	0
I/O6	Page Buffer Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O7	Data Cache Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O8	Write Protect Not Protected :1 Protected: 0	Write Protect	Write Protect	Write Protect

The Pass/Fail status on I/O1 and I/O2 is only valid during a Program/Erase operation when the device is in the Ready state.

Chip Status 1:

During a Auto Page Program or Auto Block Erase operation this bit indicates the pass/fail result.

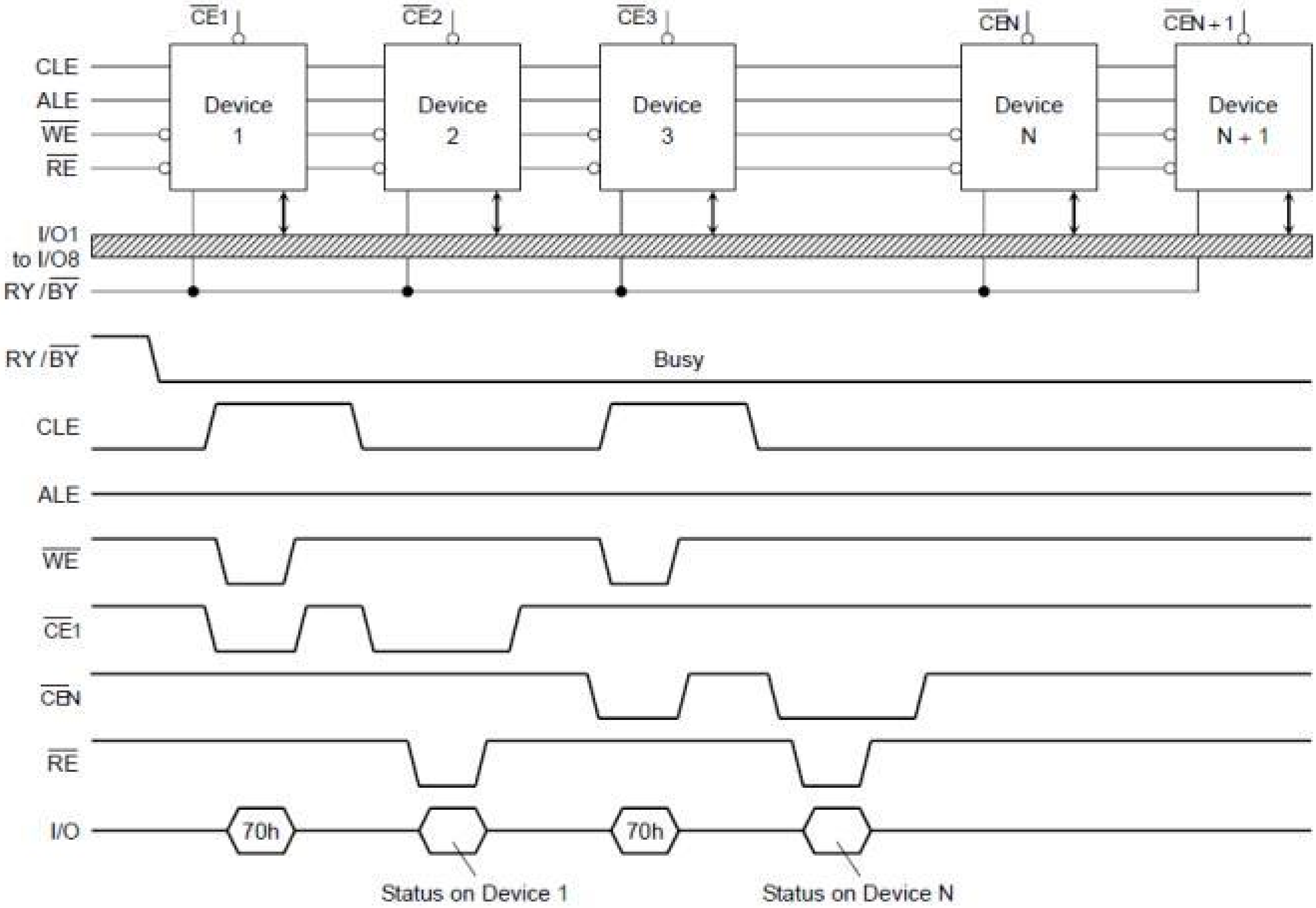
During a Auto Page Programming with Data Cache operation, this bit shows the pass/fail results of the current page program operation, and therefore this bit is only valid when I/O6 shows the Ready state.

Chip Status 2:

This bit shows the pass/fail result of the previous page program operation during Auto Page Programming with Data Cache. This status is valid when I/O7 shows the Ready State.

The status output on the I/O6 is the same as that of I/O7 if the command input just before the 70h is not 15h or 31h.

An application example with multiple devices is shown in the figure below.



System Design Note: If the RY / BY# pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

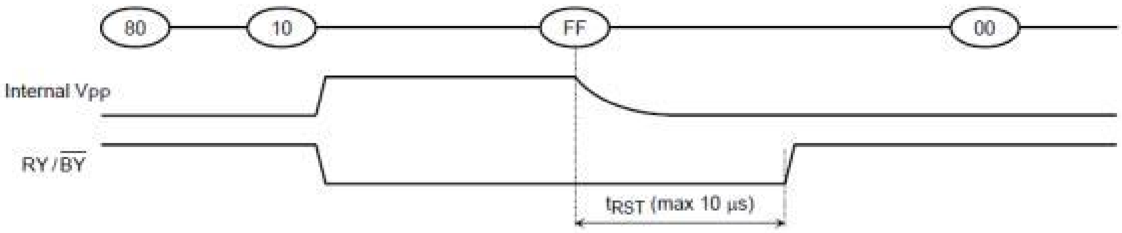
Reset

The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 volt and the device enters the Wait state.

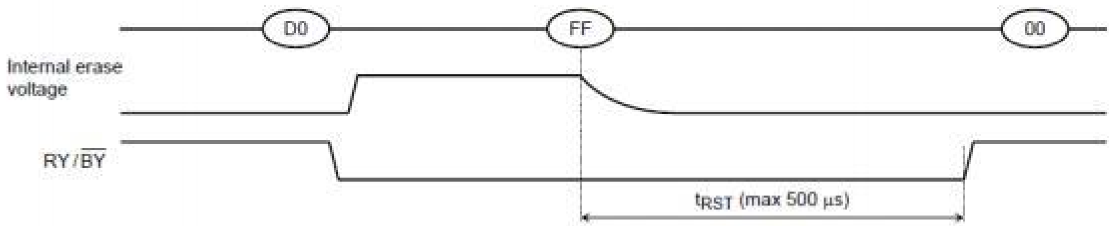
Reset during a Cache Program/Page Copy may not just stop the most recent page program but it may also stop the previous program to a page depending on when the FF reset is input.

The response to a "FFh" Reset command input during the various device operations is as follows:

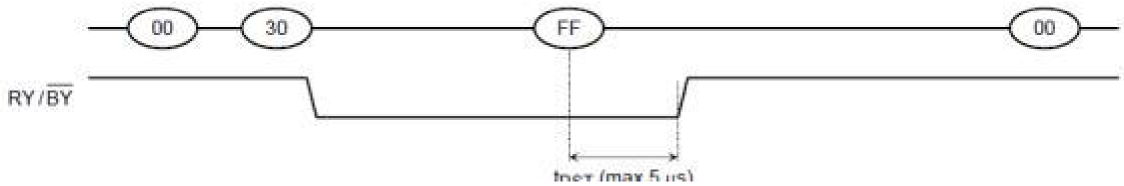
When a Reset (FFh) command is input during programming



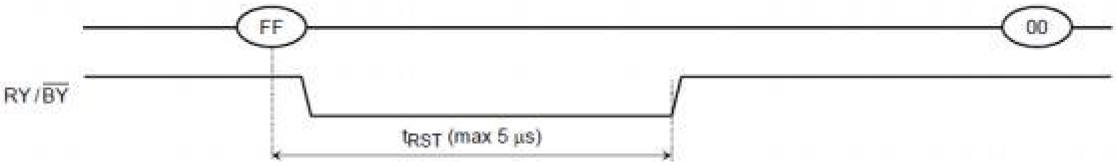
When a Reset (FFh) command is input during erasing



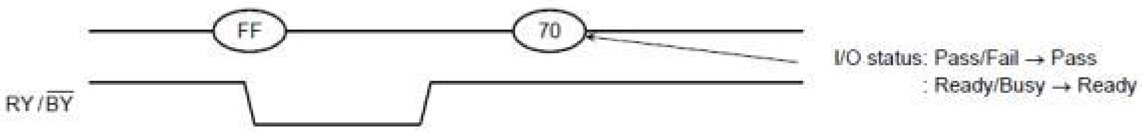
When a Reset (FFh) command is input during Read operation



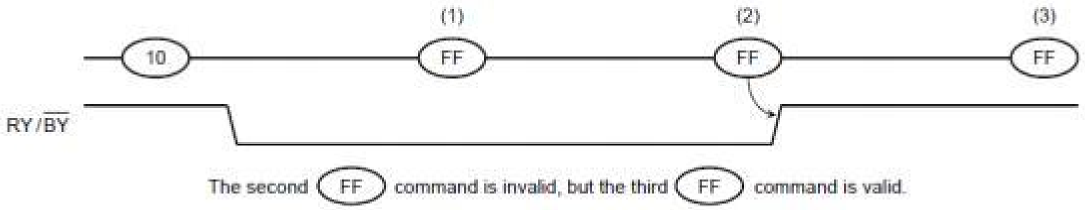
When a Reset (FFh) command is input during Ready



When a Status Read command (70h) is input after a Reset

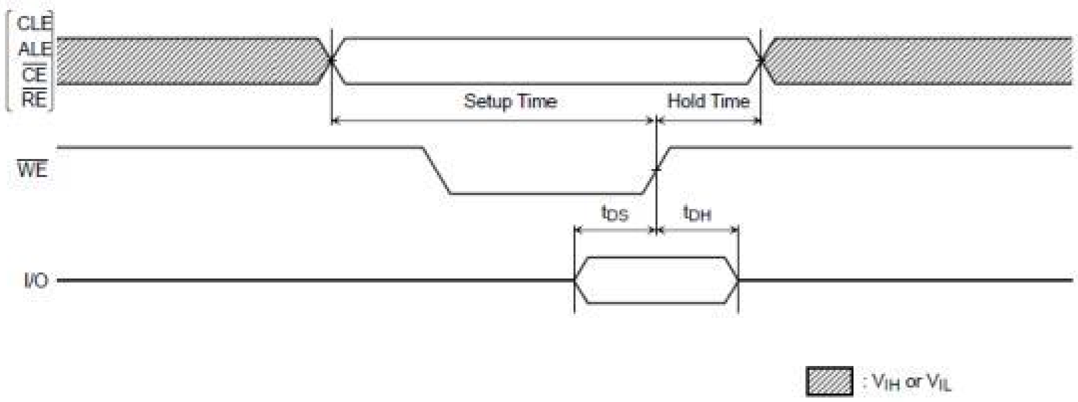


When two or more Reset commands are input in succession

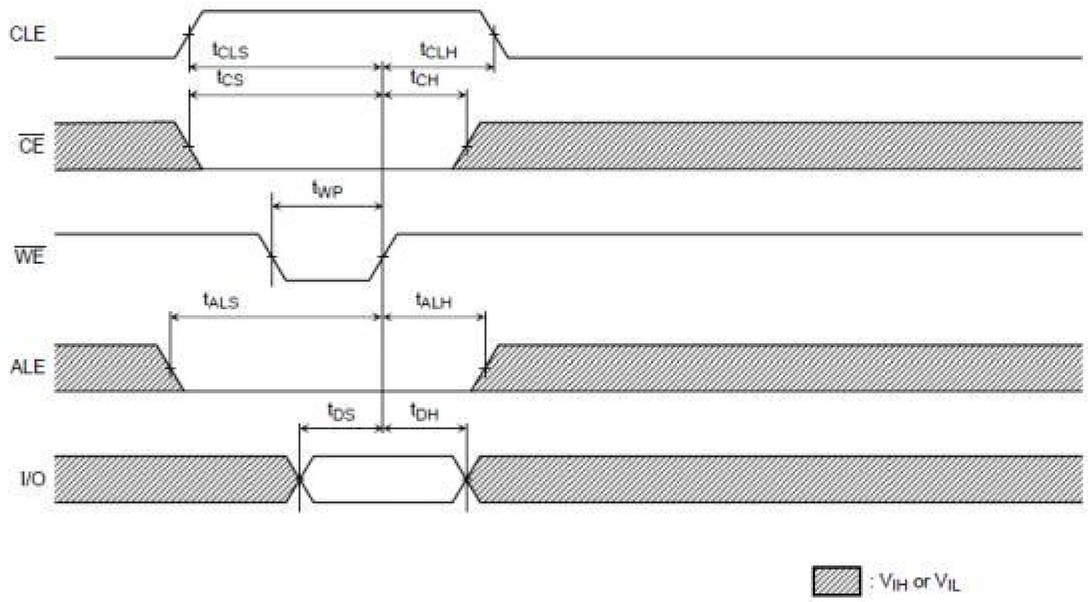


Timing Diagrams

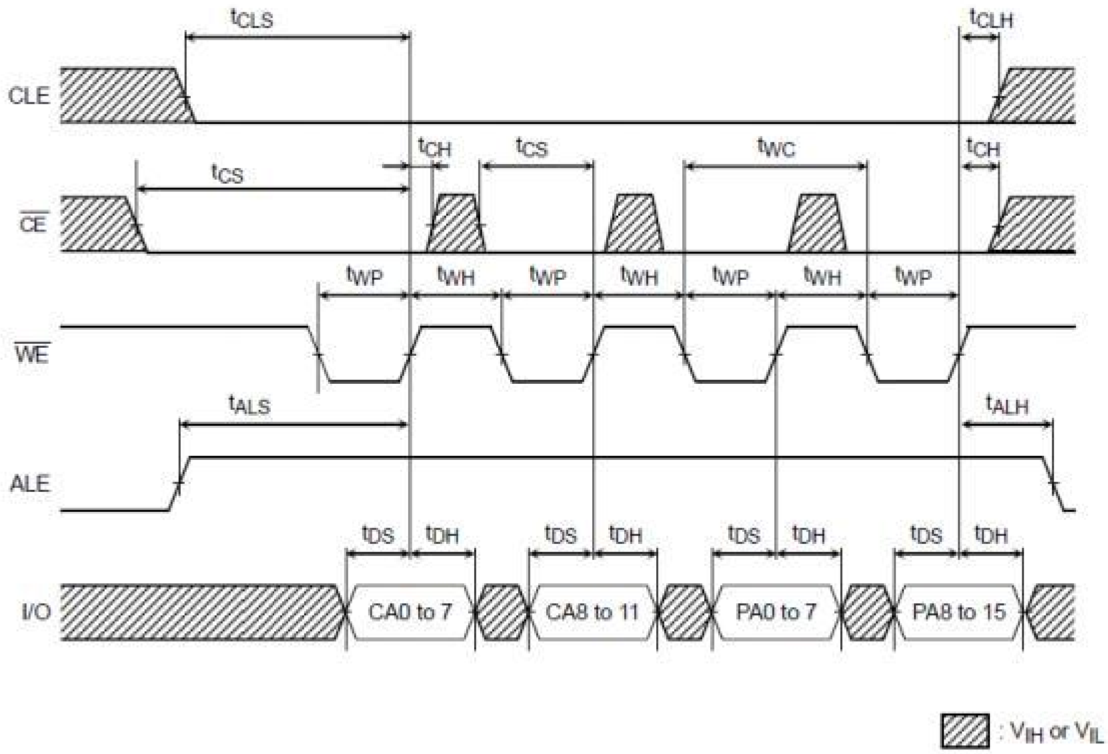
Latch Timing Diagram for Command/Address/Data



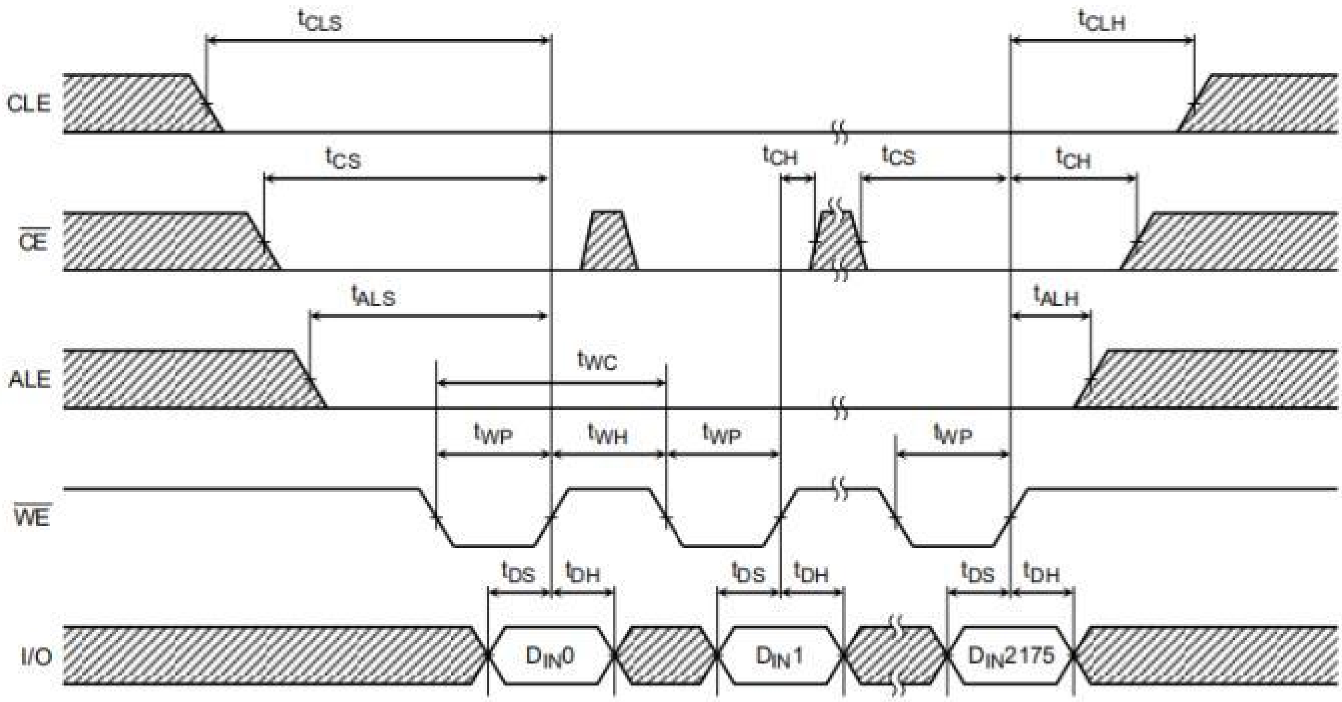
Command Input Cycle Timing Diagram



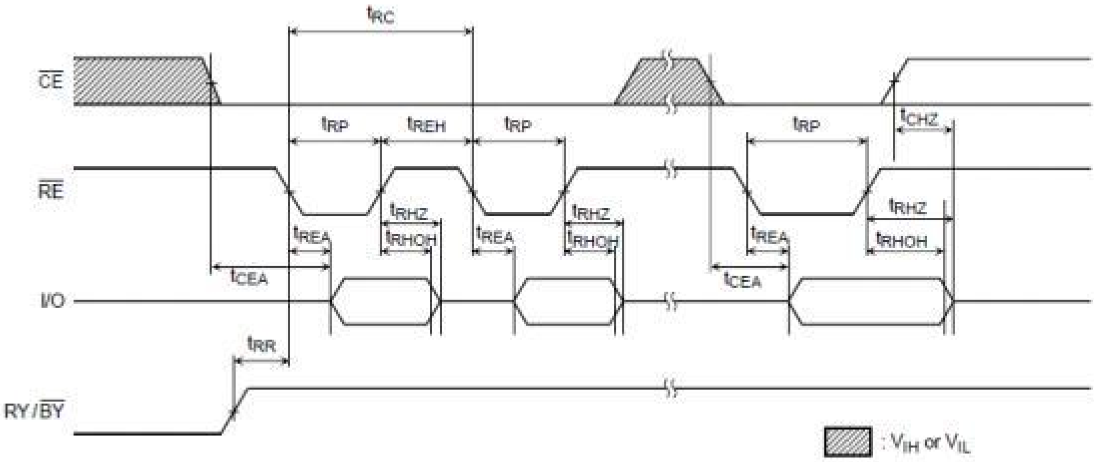
Address Input Cycle Timing Diagram



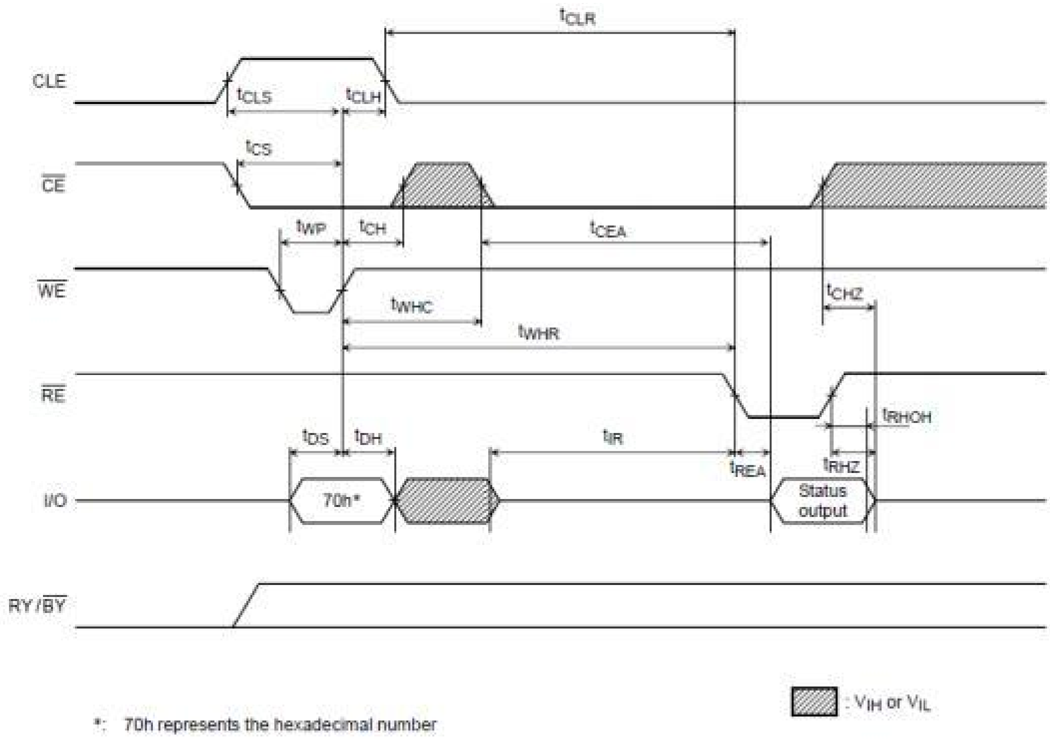
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram

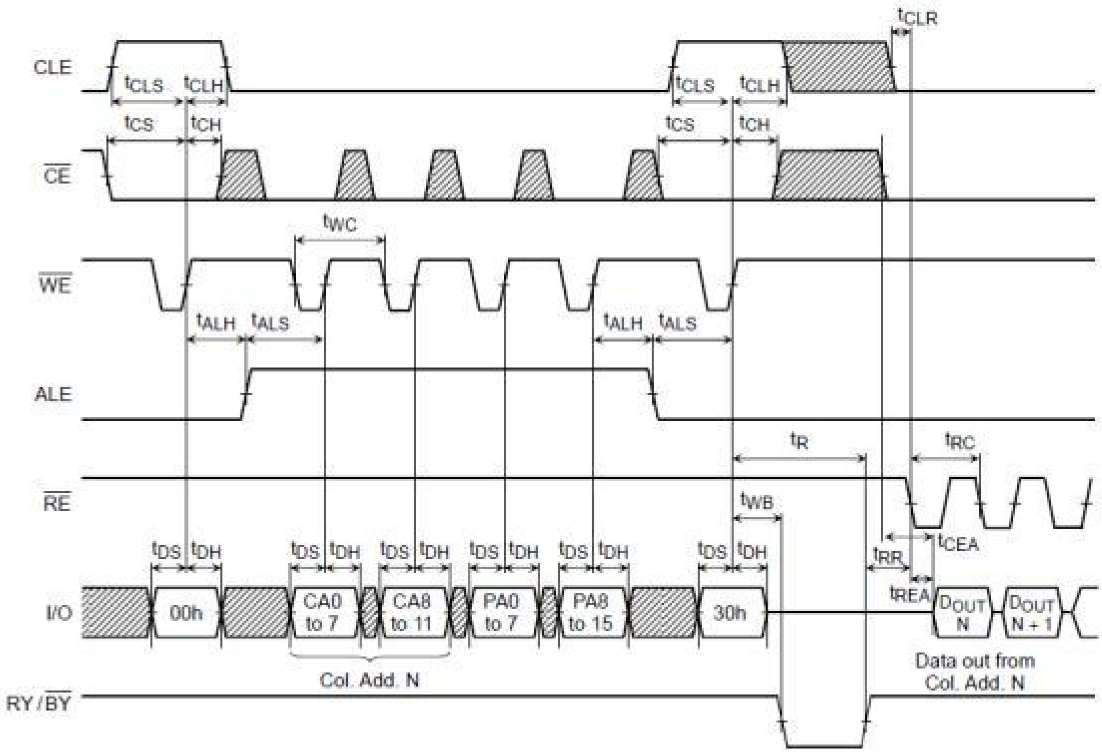


Status Read Cycle Timing Diagram

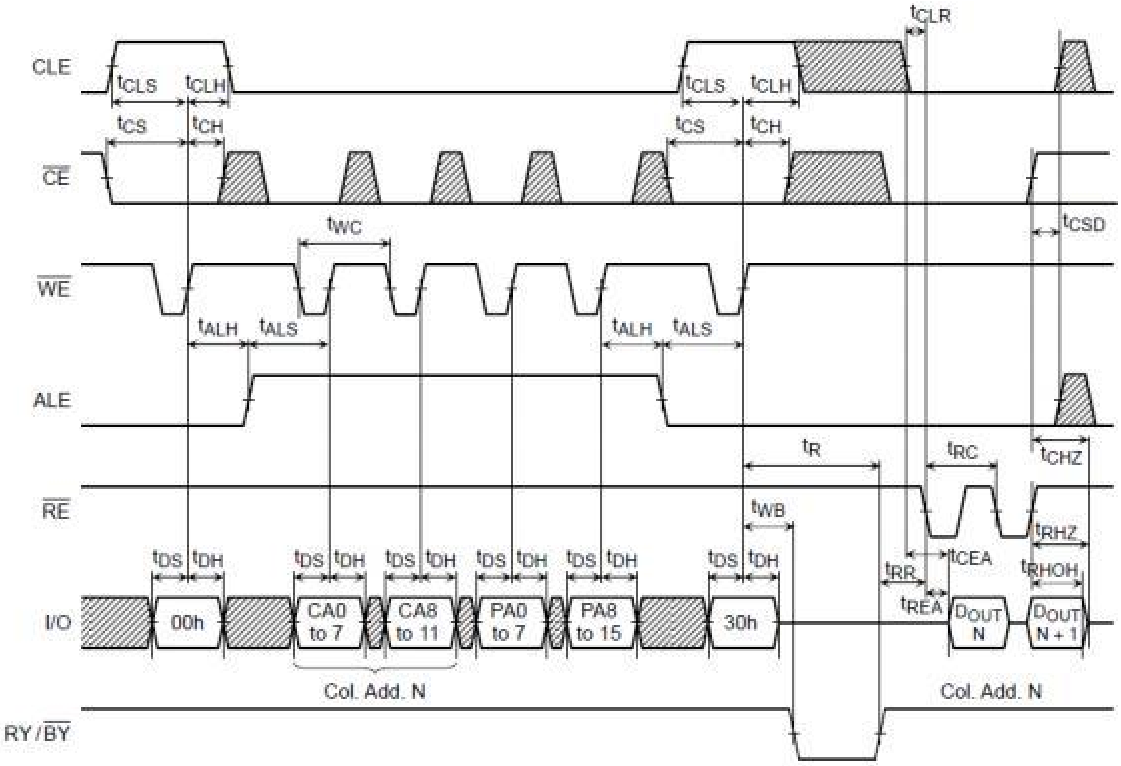


*: 70h represents the hexadecimal number

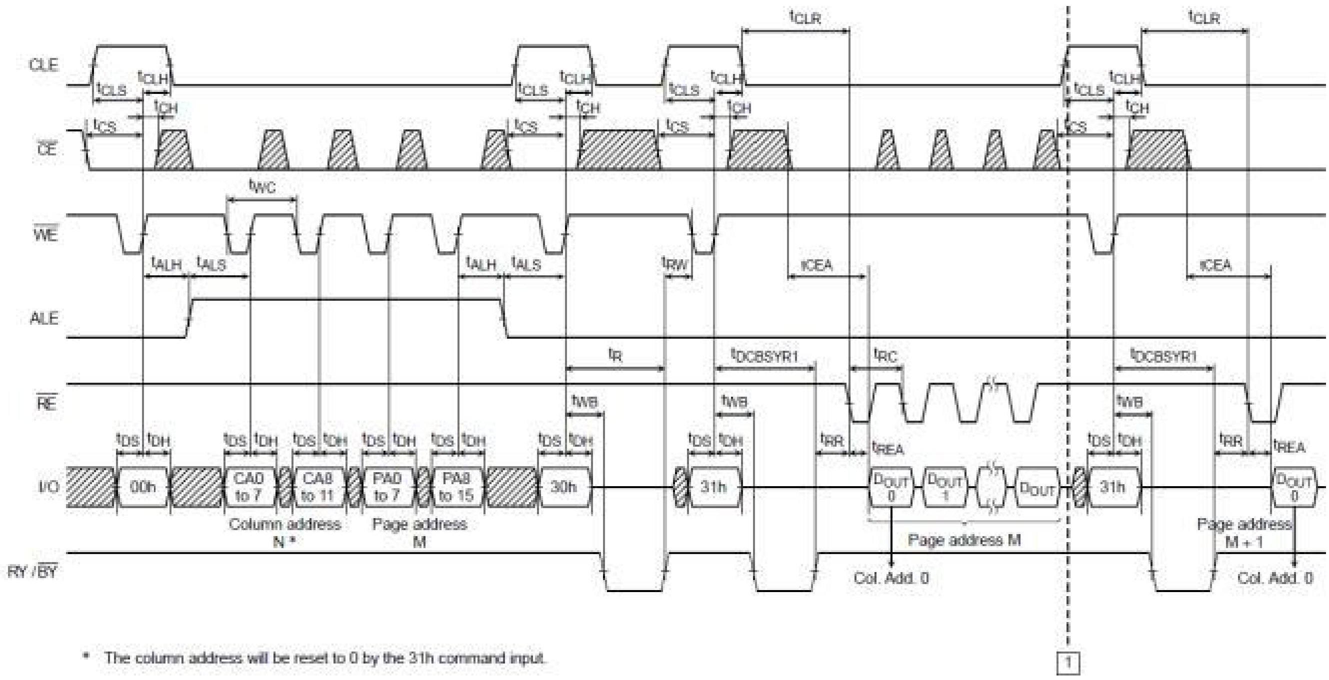
Read Cycle Timing Diagram



Read Cycle Timing Diagram: When Interrupted by /CE



Read Cycle with Data Cache Timing Diagram (1/2)



* The column address will be reset to 0 by the 31h command input.

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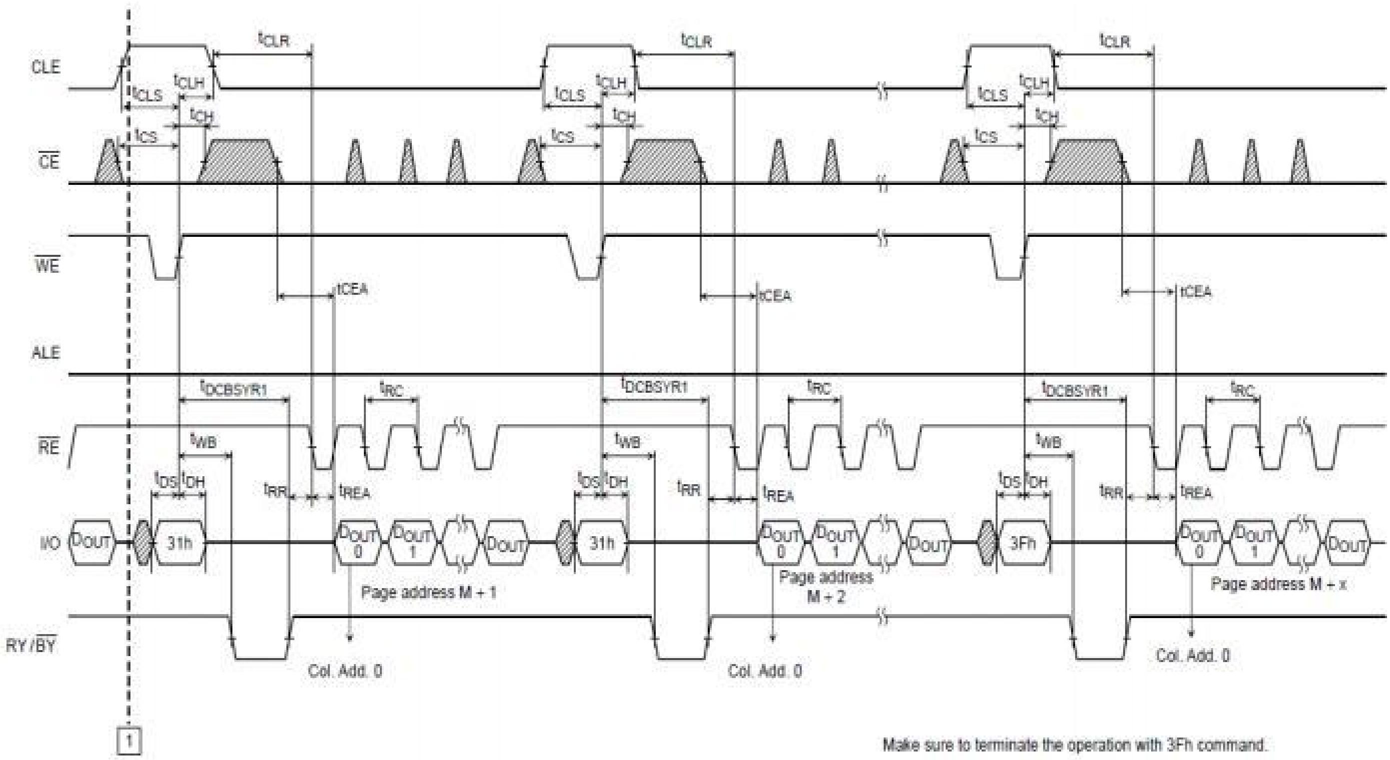
Read Cycle with Data Cache Timing Diagram (2/2)



Make sure to terminate the operation with 3Fh command.

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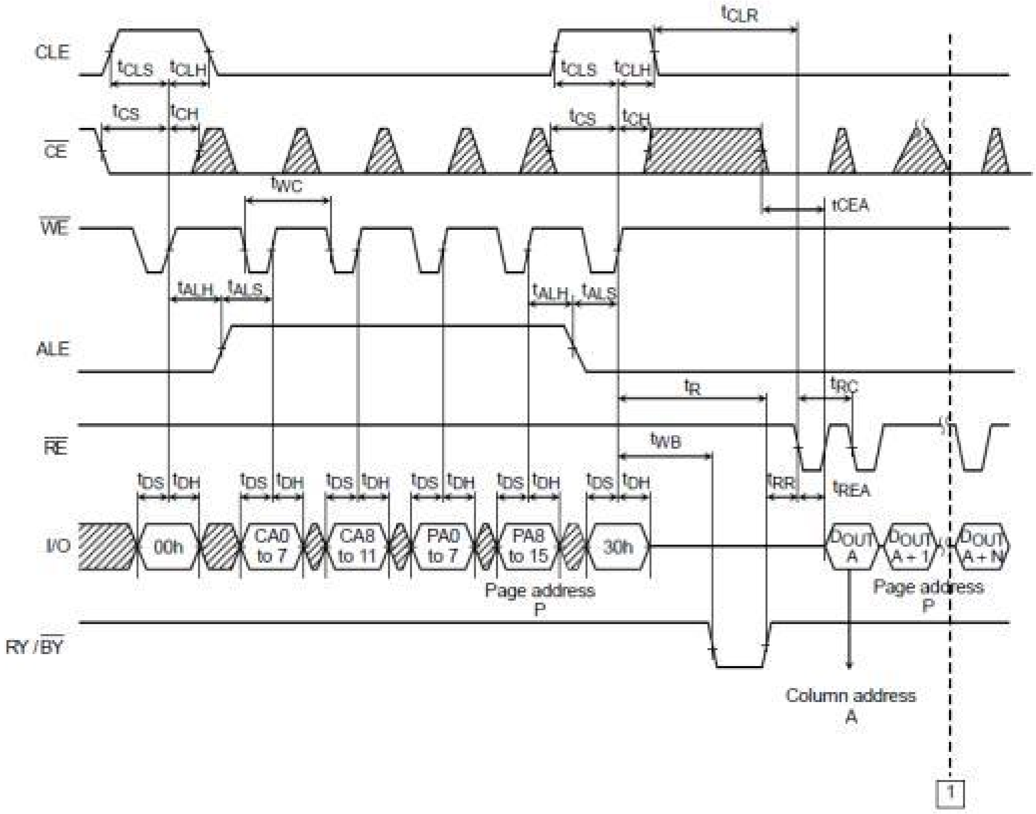
Column Address Change in Read Cycle Timing Diagram (1/2)



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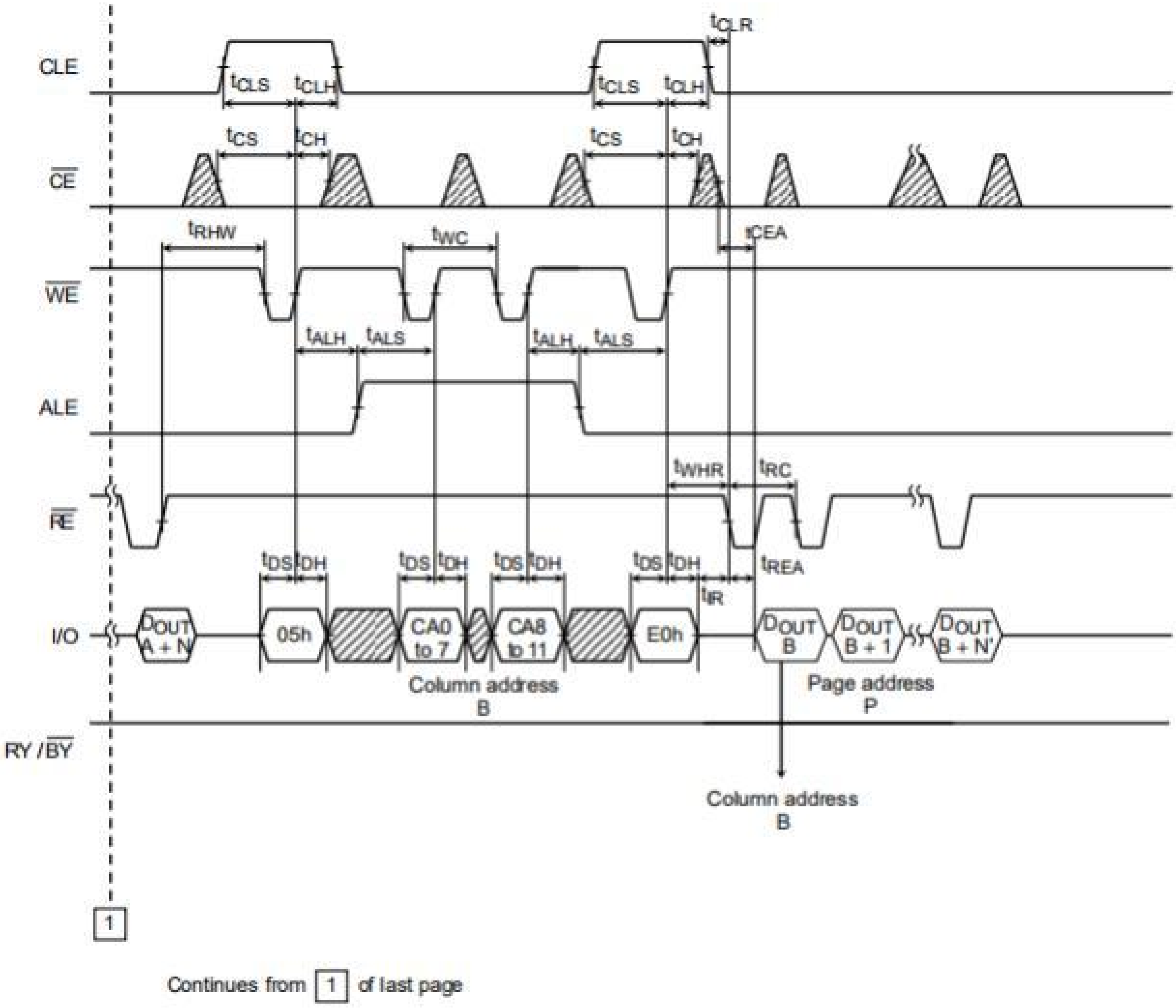
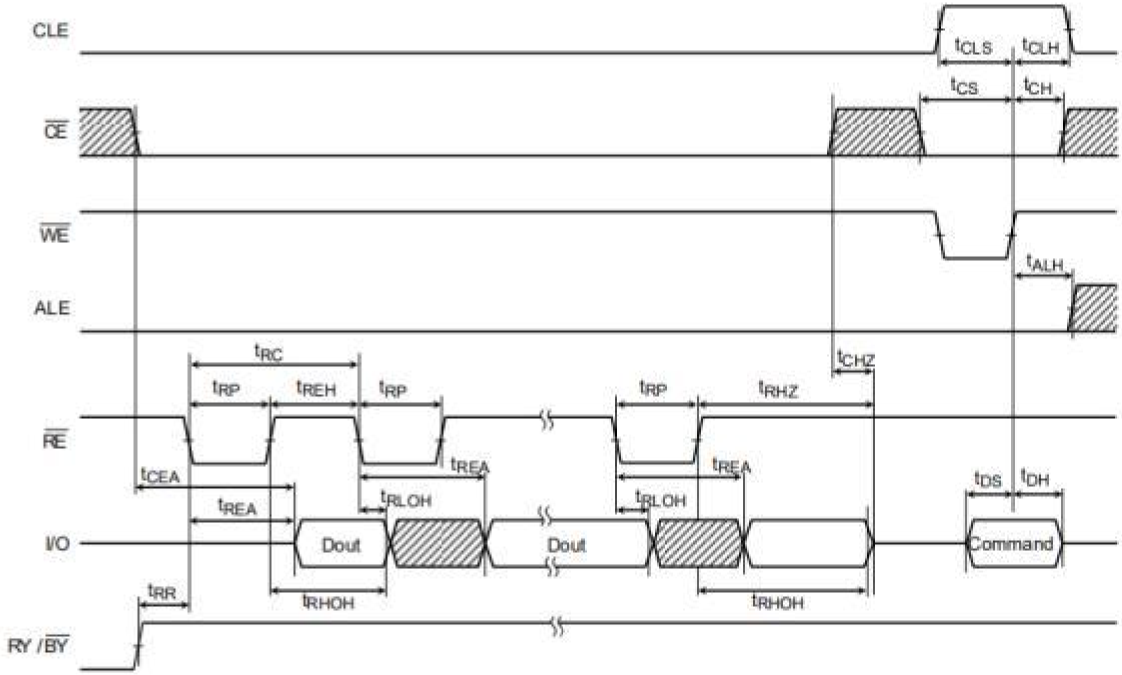
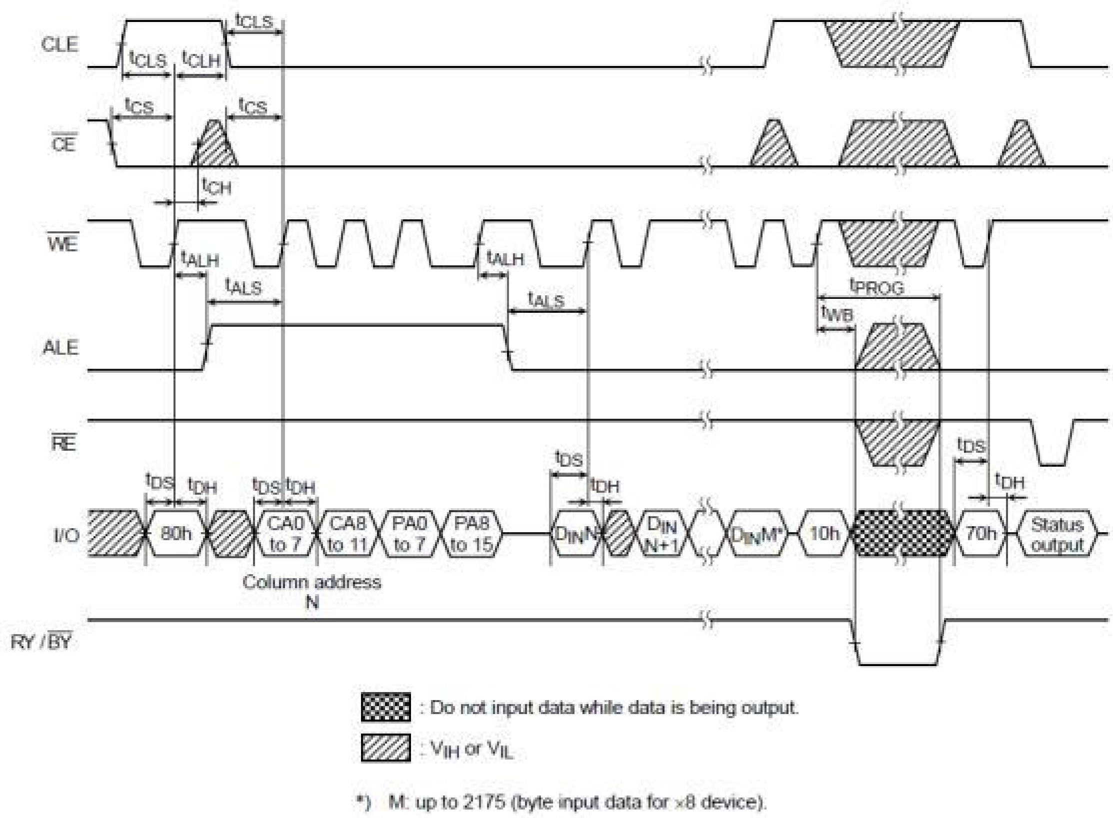
Column Address Change in Read Cycle Timing Diagram (2/2)



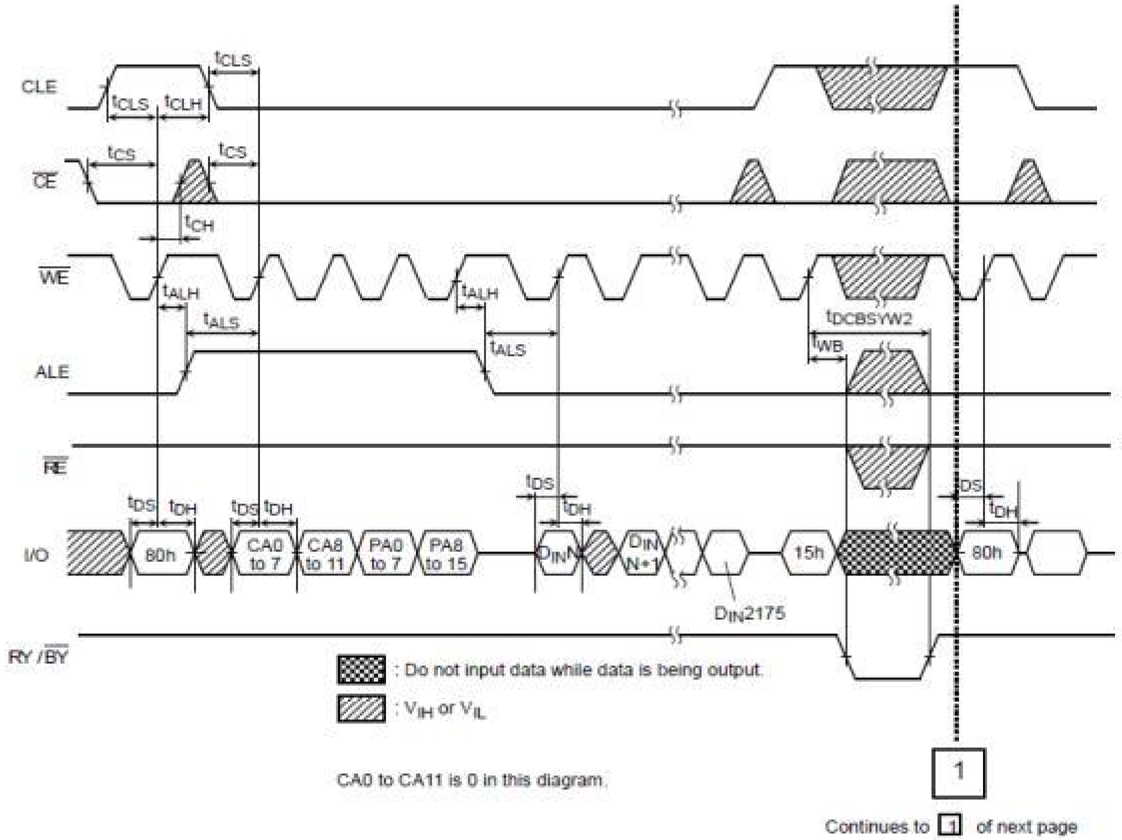
Data Output Timing Diagram



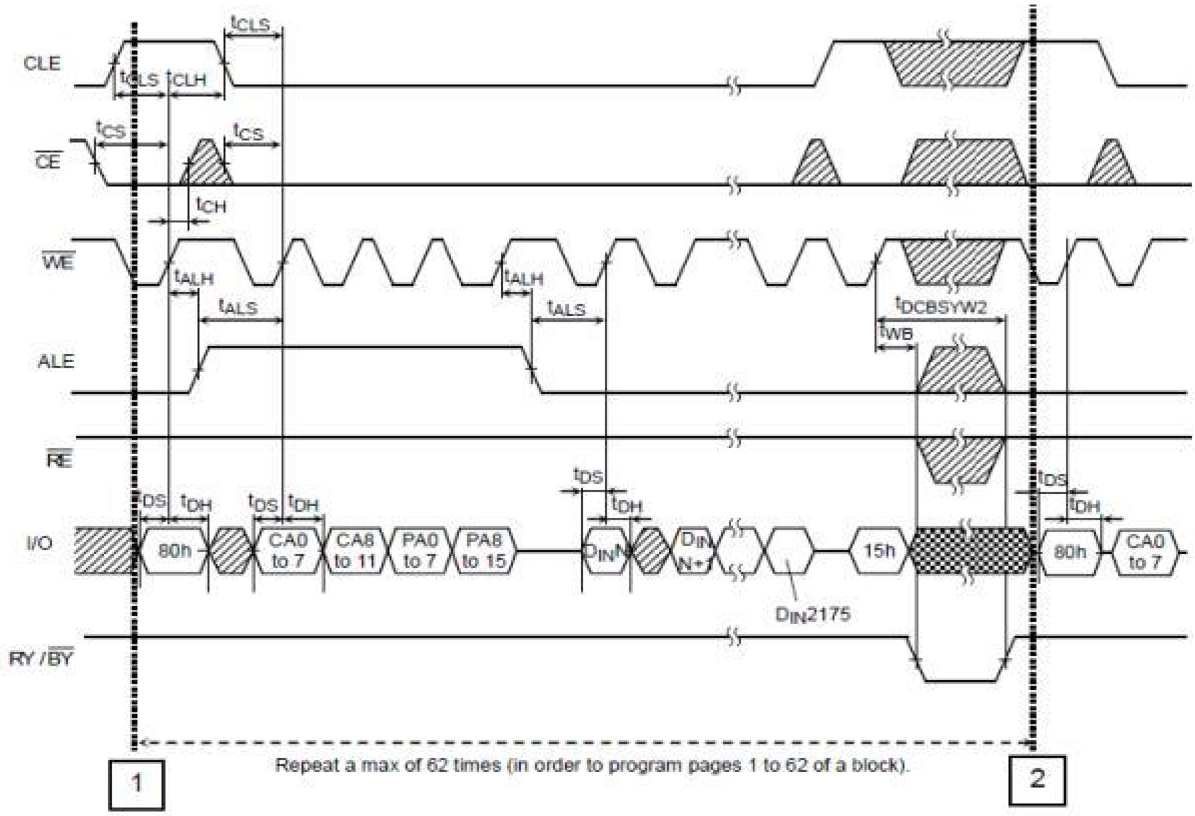
Auto-Program Operation Timing Diagram



Auto-Program Operation with Data Cache Timing Diagram (1/3)



Auto-Program Operation with Data Cache Timing Diagram (2/3)



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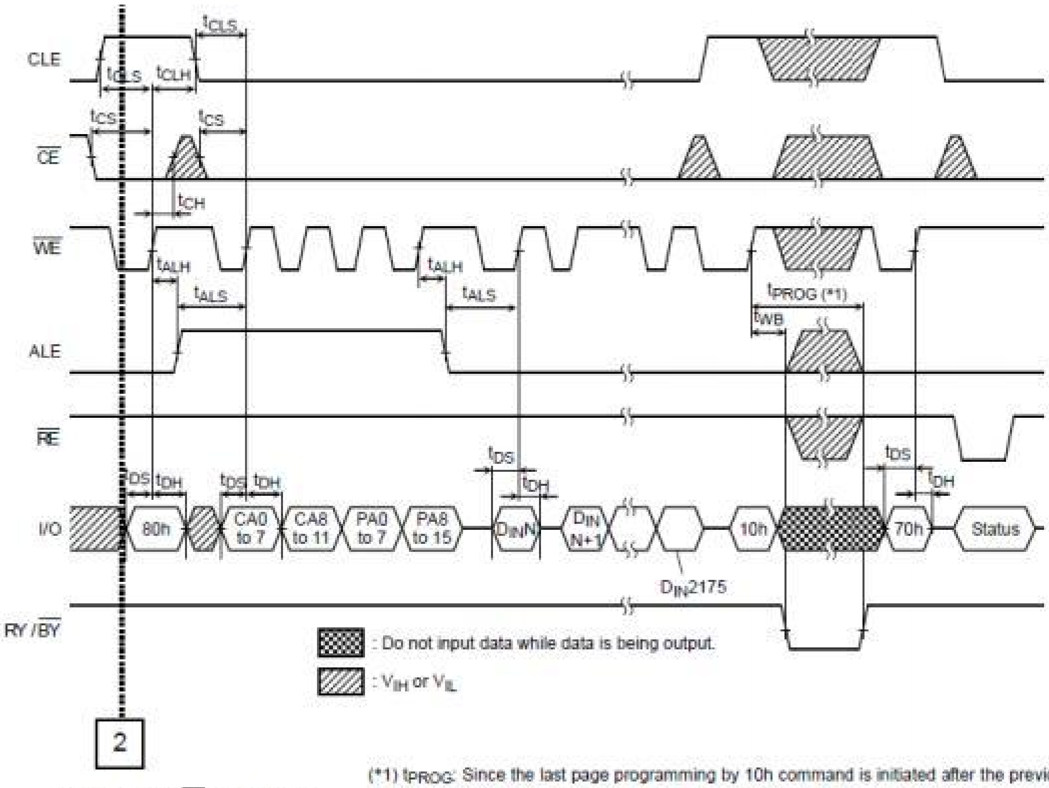
: Do not input data while data is being output.

: V_{IH} or V_{IL}

Auto-Program Operation with Data Cache Timing Diagram (3/3)



Continued from 2 of last page

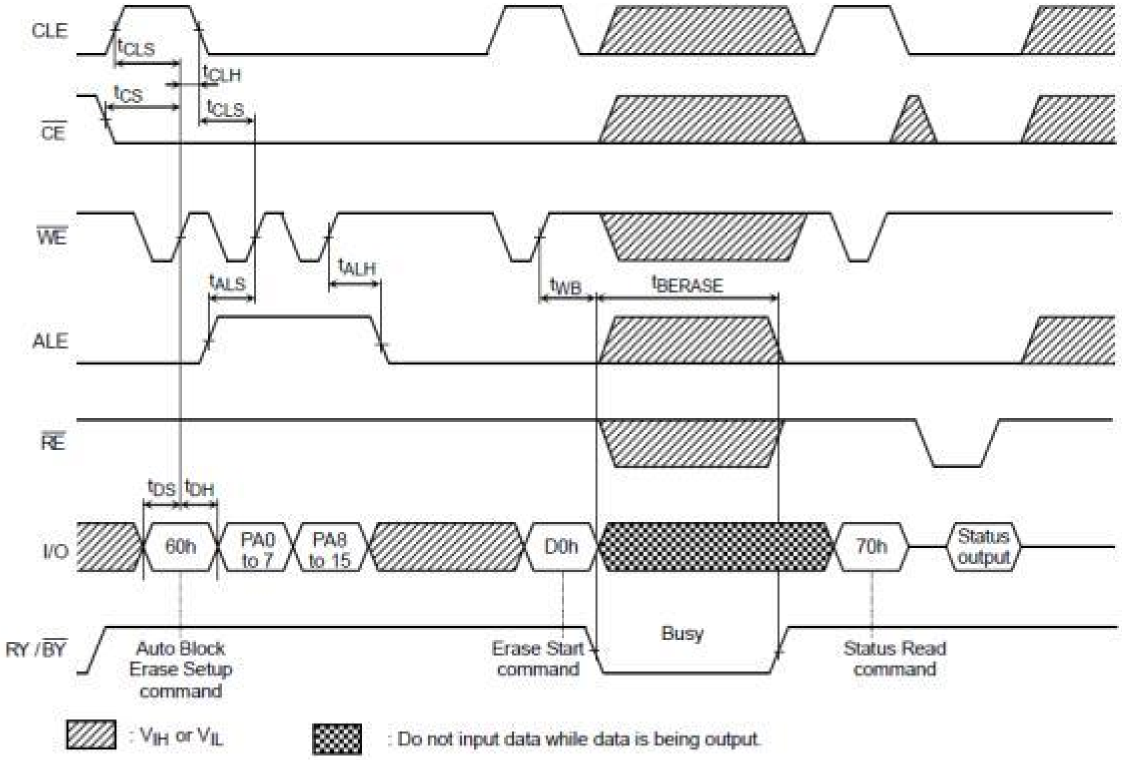
(*1) t_{PROG}: Since the last page programming by 10h command is initiated after the previous cache program, the t_{PROG} during cache programming is given by the following equation.

t_{PROG} = t_{PROG} of the last page + t_{PROG} of the previous page – A
A = (command input cycle + address input cycle + data input cycle time of the last page)

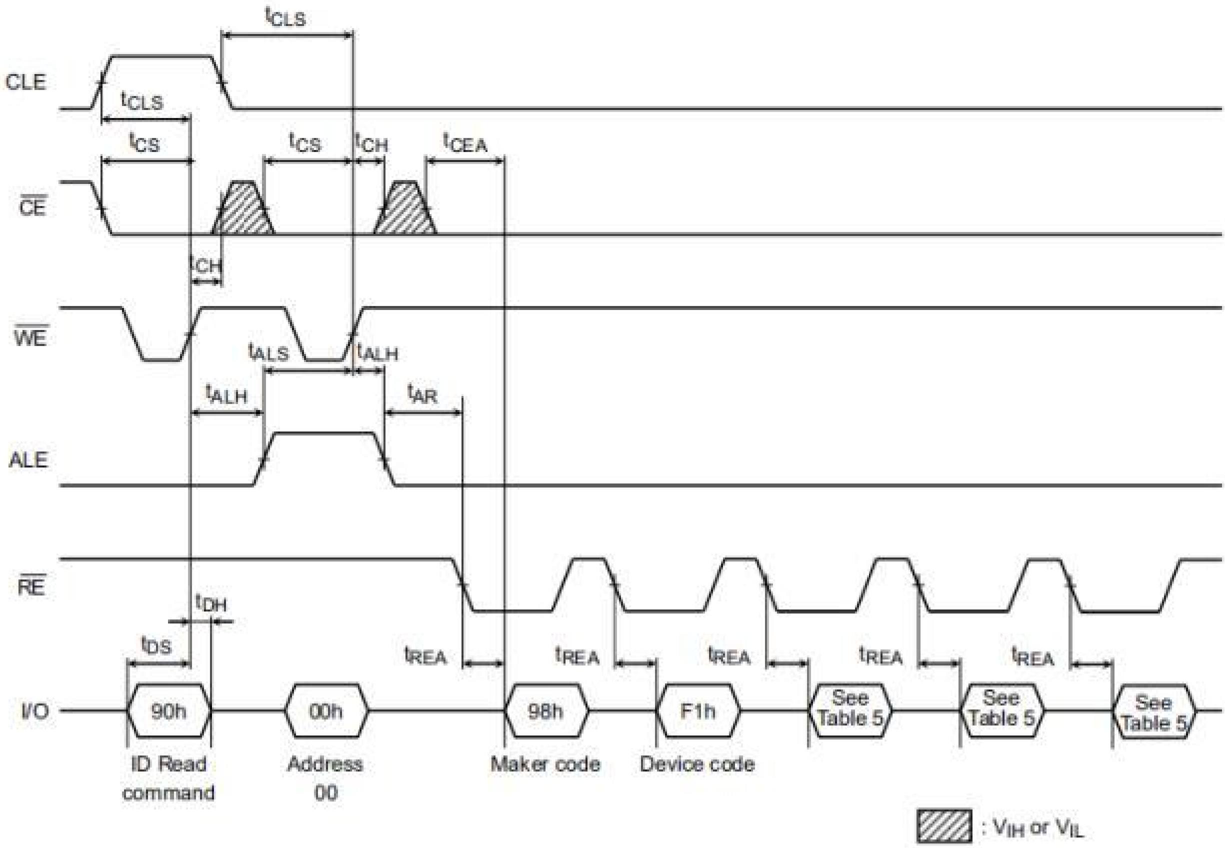
If "A" exceeds the t_{PROG} of previous page, t_{PROG} of the last page is t_{PROG} max.

(Note) Make sure to terminate the operation with 80h-10h- command sequence. If the operation is terminated by 80h-15h command sequence, monitor I/O 6 (Ready / Busy) by issuing Status Read command (70h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.

Auto Block Erase Timing Diagram



ID Read Operation Timing Diagram



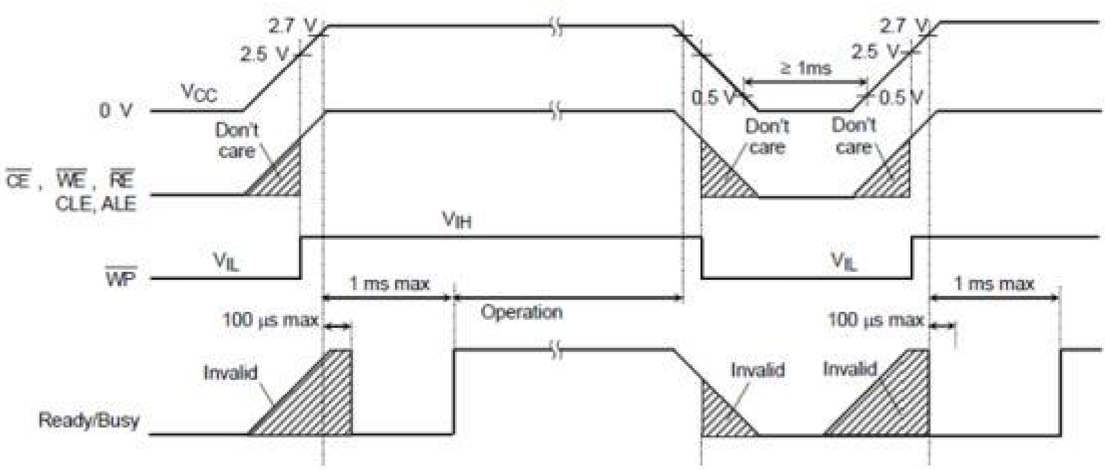
Application Notes and Comments

(1) Power-on/off sequence:

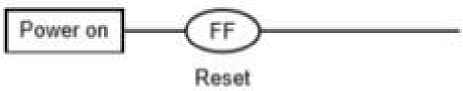
The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h.

The WP signal is useful for protecting against data corruption at power-on/off.



(2)Power-on Reset The following sequence is necessary because some input signals may not be stable at power-on.



(3) Prohibition of unspecified commands

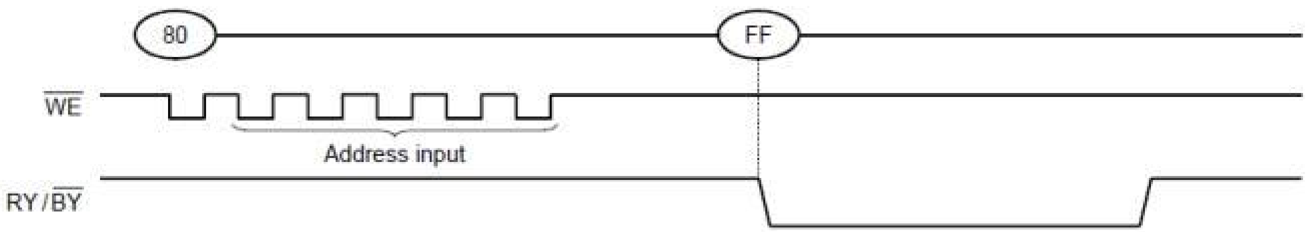
The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(4) Restriction of commands while in the Busy state

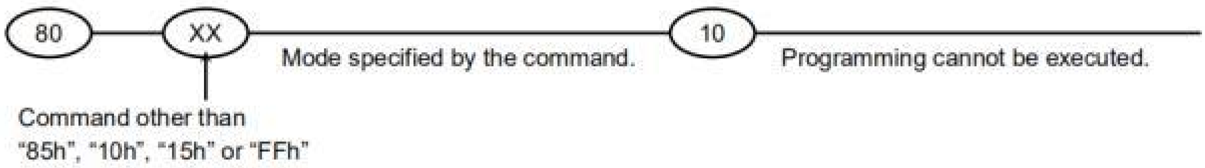
During the Busy state, do not input any command except 70hand FFh.

(5) Acceptable commands after Serial Input command "80h"

Once the Serial Input command "80h" has been input, do not input any command other than the Column Address Change in Serial Data Input command "85h", Auto Program command "10h", Auto Program with Data Cache Command "15h", or the Reset command "FFh".

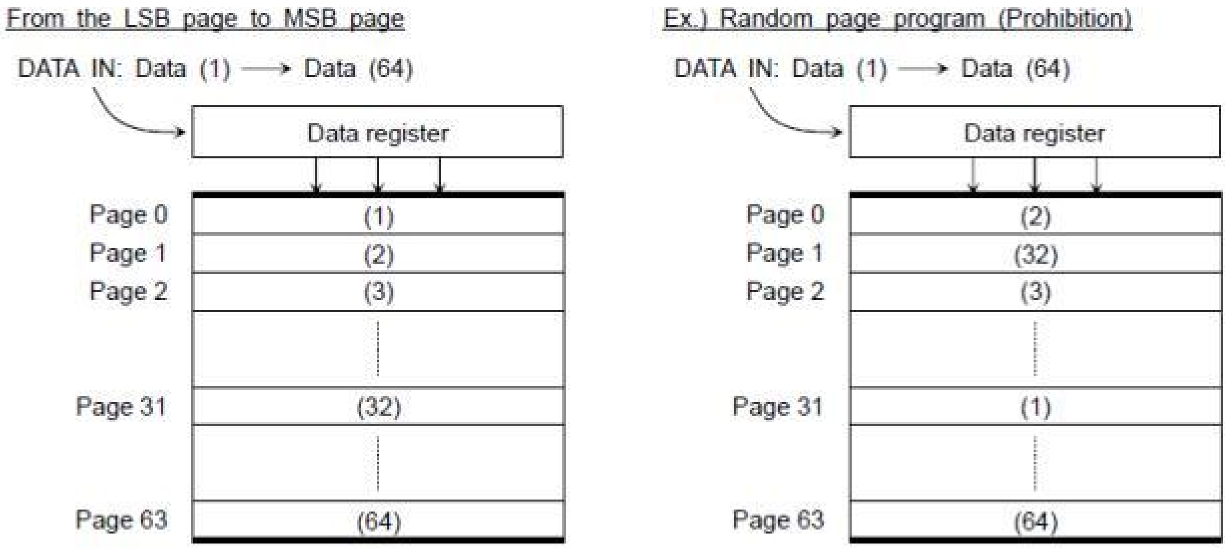


If acommand other than "85h" , "10h" , "15h" or "FFh" is input, the Program operation is not performed and the device operation is set to the mode which the input command specifies.

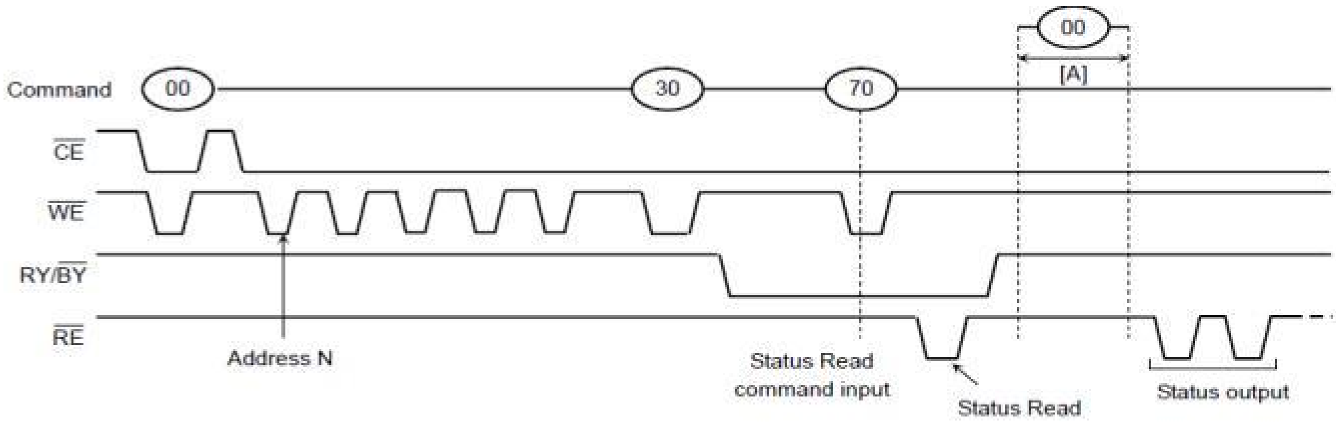


(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

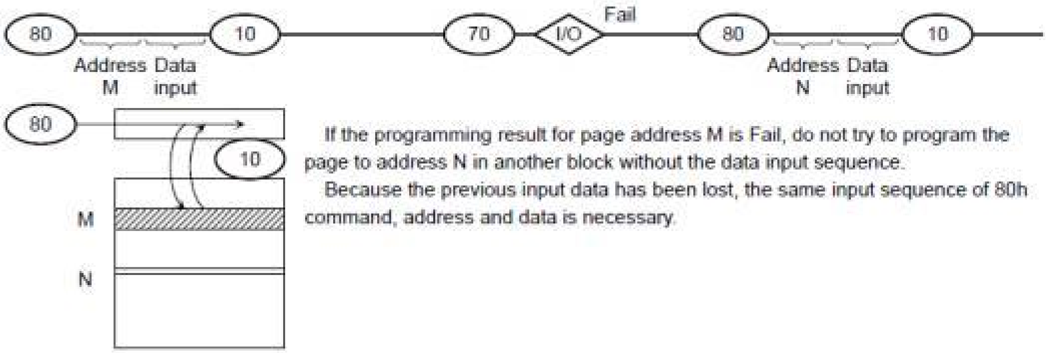


(7) Status Read during a Read operation



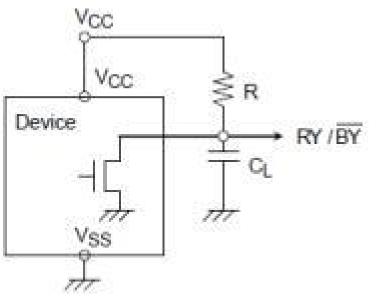
The device status can be readout by inputting the Status Read command "70h" in Read mode. Once the device has been set to Status Read mode by a "70h" command, the device will not return to Read mode unless the Read command "00h" is inputted during [A]. If the Read command "00h" is inputted during [A], Status Read mode is reset, and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

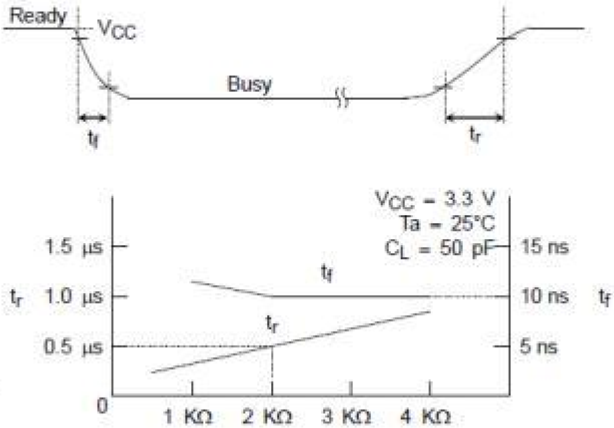
(8) Auto programming failure



If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence.
Because the previous input data has been lost, the same input sequence of 80h command, address and data is necessary.

(9) RY / BY# : termination for the Ready/Busy pin (RY / BY#)
A pull-up resistor needs to be used for termination because the RY / BY# buffer consists of an open drain circuit.



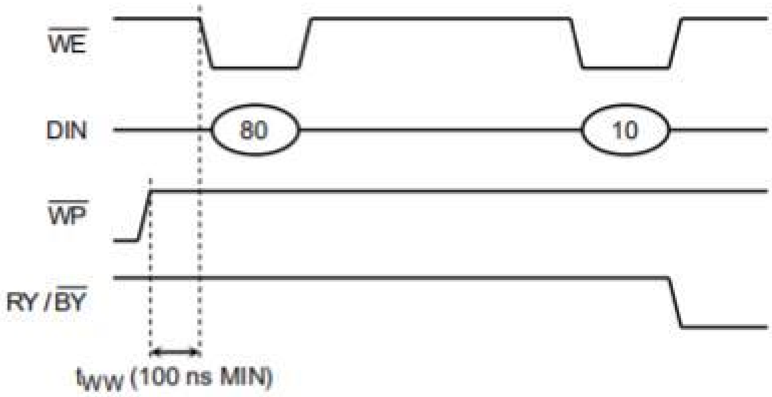


This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.

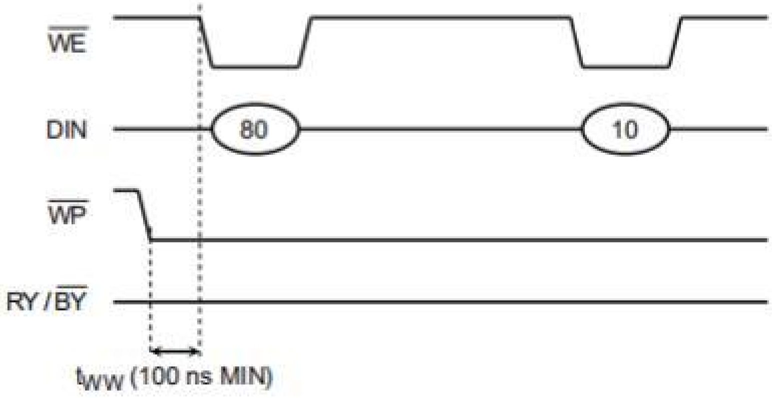
(10) Note regarding the WP# signal

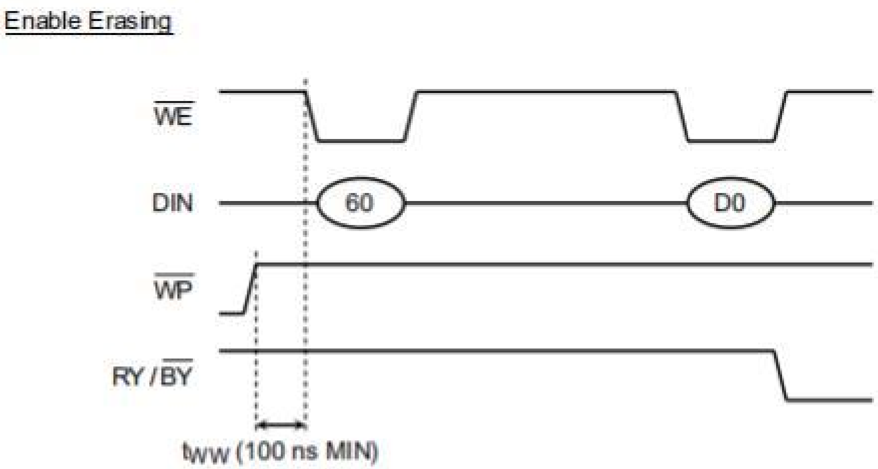
The Erase and Program operations are automatically reset when WP# goes Low. The operations are enabled and disabled as follows:

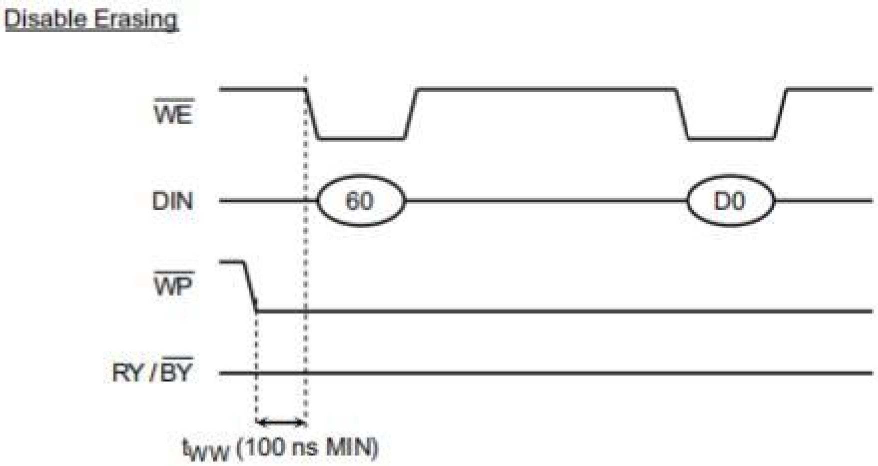
Enable Programming



Disable Programming



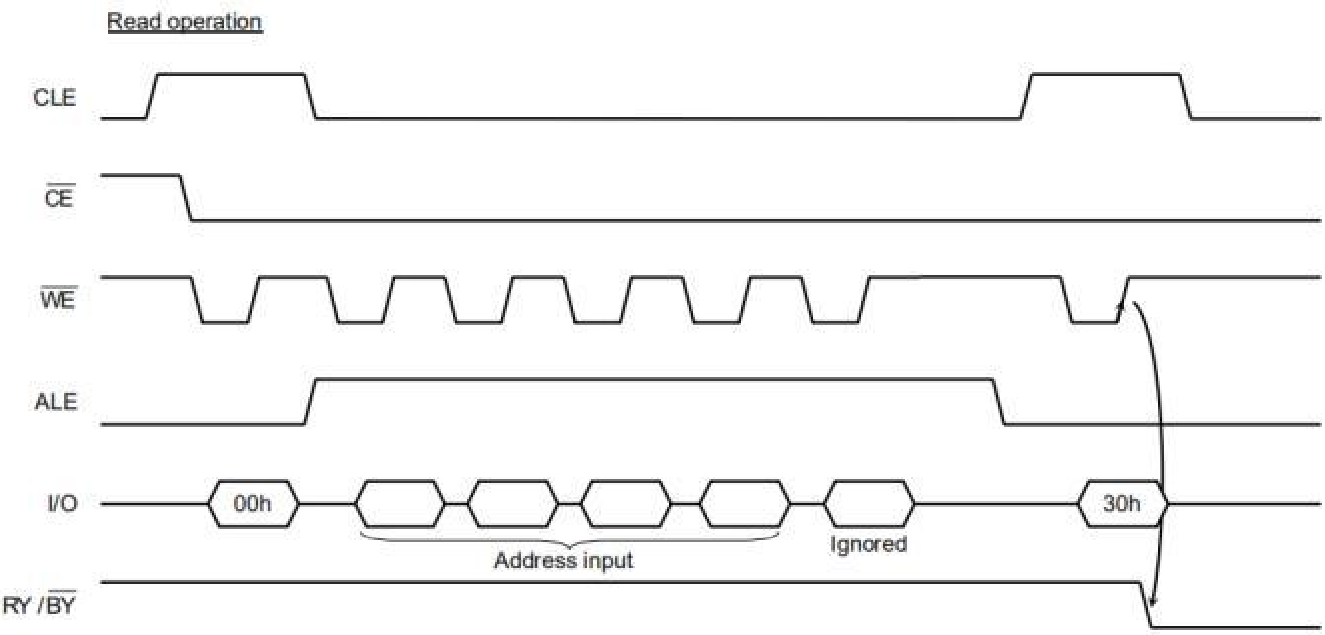




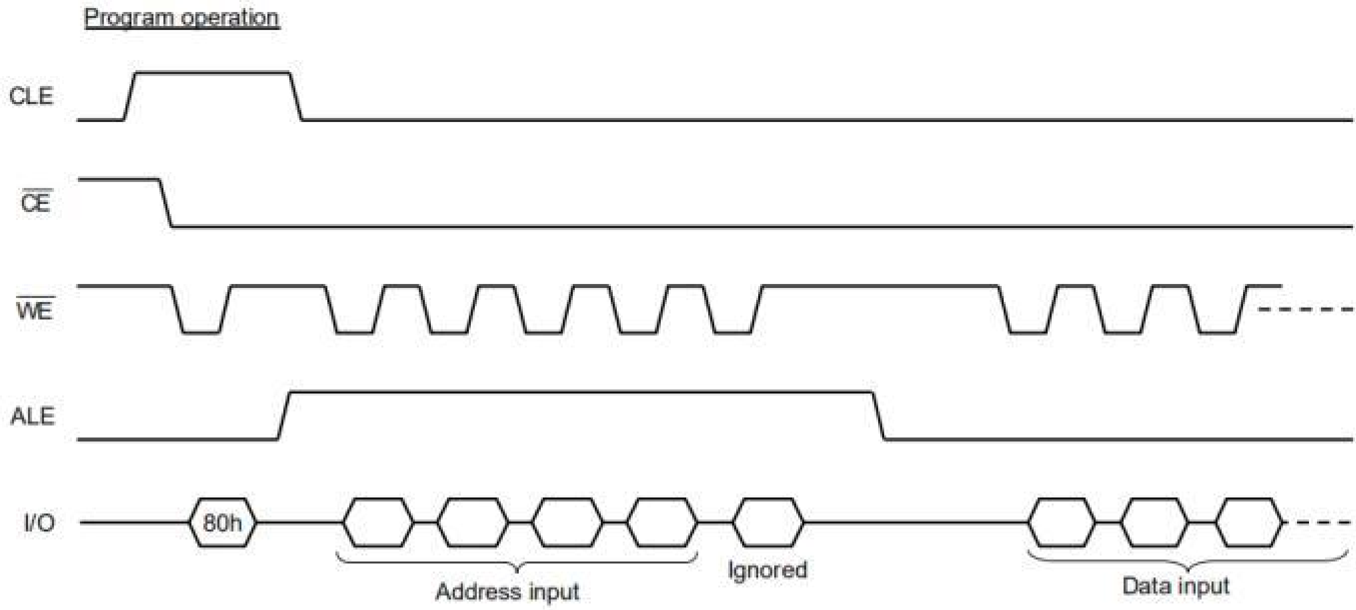
(11) When five address cycles are input

Although the device may read in a fifth address, it is ignored inside the chip.

Read operation

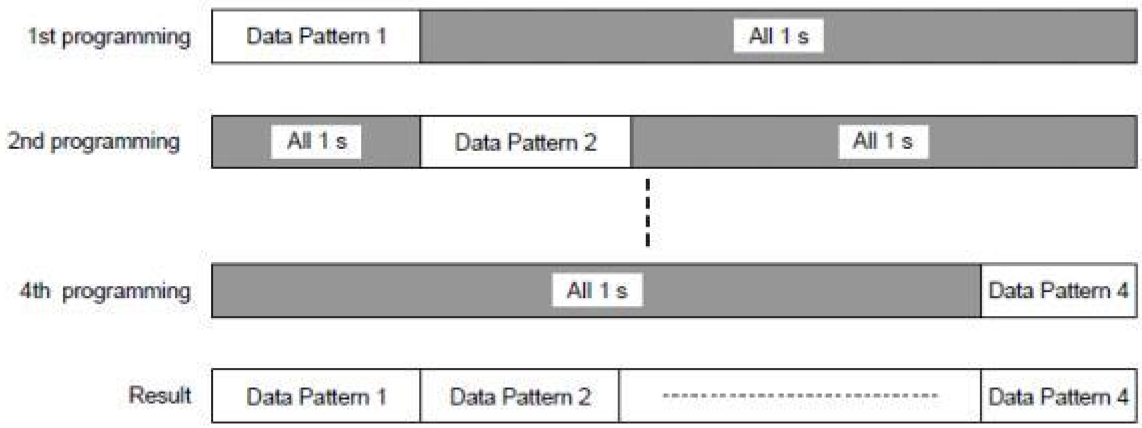


Program operation



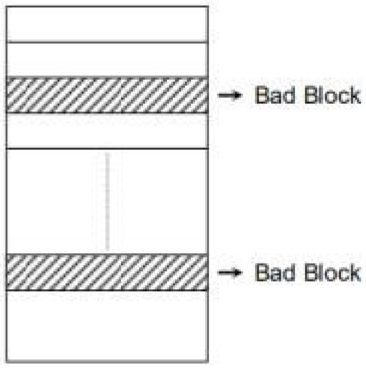
(12) Several programming cycles on the same page (Partial Page Program)

Each segment can be programmed individually as follows:



(13) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.

Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

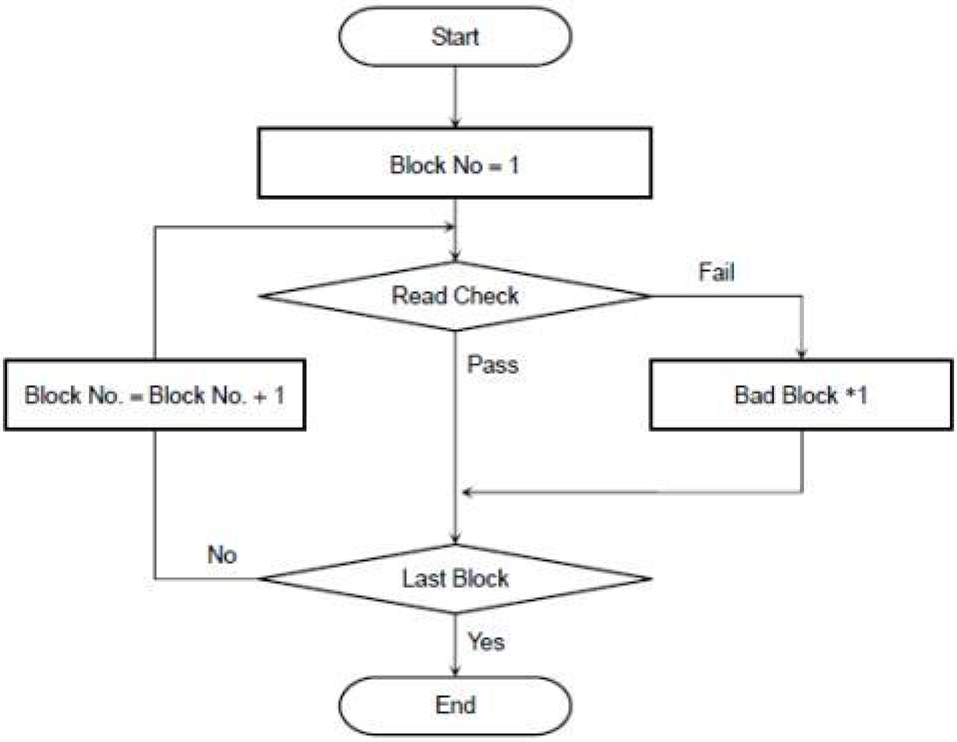
The number of valid blocks over the device lifetime is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	1004	—	1024	Block

Bad Block Test Flow

Regarding invalid blocks, bad block mark is in whole pages.

Please read one column of any page in each block. If the data of the column is 00(Hex), define the block as a bad block.



*1: No erase operation is allowed to detected bad blocks

(14) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.

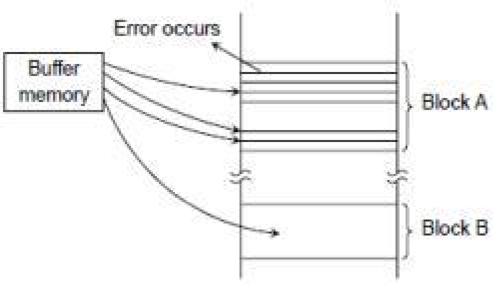
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Read	Bit Error	ECC Correction / Block Refresh

. ECC: Error Correction Code. 8 bit correction per 512 Bytes is necessary.

. Block Replacement

Program



When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(15) Do not turnoff the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

(16) Reliability Guidance

This reliability guidance is intended to notify some guidance related to using NAND flash with 8 bit ECC for each 512 bytes. For detailed reliability data, please refer to ZETTA's reliability note. Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes may be recovered by a block erase.

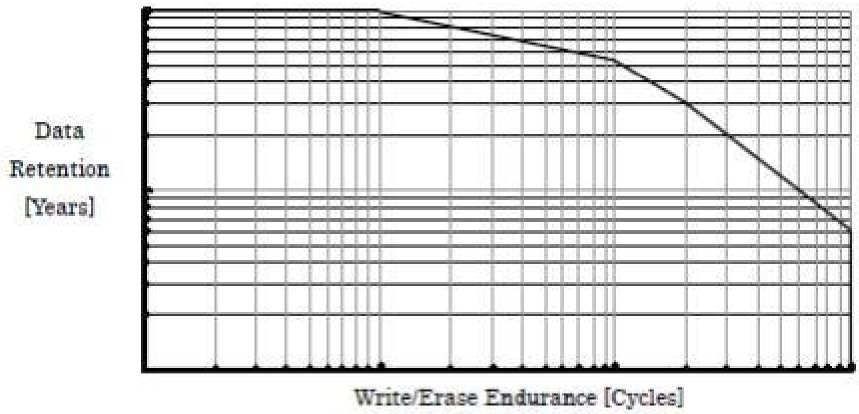
ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

. Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

. Data Retention

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again. Here is the combined characteristics image of Write/Erase Endurance and Data Retention.



Read Disturb

A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

Part Numbering System

ZDND XX XX X X X - X X

Package
A: 12 x 20 mm2 (TSOP1 48) H-ROHS & Halogen Free
F: 6 x 8 mm2 (BGA24)

Temperature
E: Extended (-25°C~85°C)
I: Industrial (-40°C~85°C)

Versions
A:Versions A
B:Versions B

Classification
1: SLC Small Block
2: MLC Small Block
3: SLC Large Block
4: MLC Large Block

Operation Voltage
U: 3.3V

Organization
08: x8

Device Density
1G: 1Gbit

Base Part Number
ZDND: Zetta Nand Flash Family

Revision History:

Rev.	Date	Changes	Remark
1.0	2023/8/15	Initial version	Preliminary
1.1	2023/12/28	Package update	Preliminary